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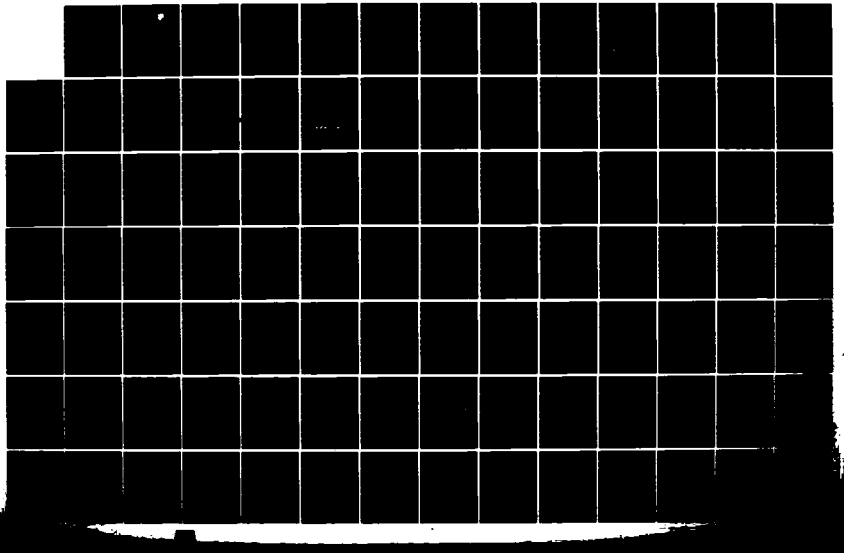

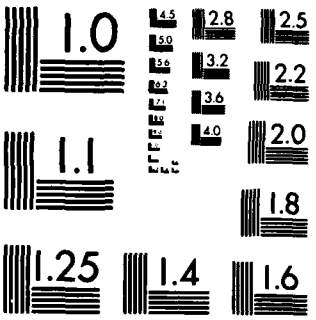

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September 1984

ELECTRICAL OVERSTRESS PROTECTION OF SUBMICRON DEVICES

BDM Corporation

Robert J. Antinone and Phillip A. Young

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

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APPROVED: Daniel J. Burns

DANIEL J. BURNS
Project Engineer

APPROVED: W. S. Tuthill

W. S. TUTHILL, Colonel, USAF
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John A. Ritz

JOHN A. RITZ
Acting Chief, Plans Office

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The objective of this program was to further define the electrical overstress (EOS) sensitivity characterization procedures for microelectric devices and to investigate the EOS sensitivity of micron and submicron linewidth circuit structures. Another objective was to investigate improved EOS protection schemes and evaluate their benefits versus performance and cost penalties.

The approach chosen to achieve these objectives was to attempt to design input protection networks which would protect an MOS device fabricated from a submicron process from an electrostatic discharge (ESD) threat. The program included the definition of ESD threats, examination of the characteristics of existing input protection networks, a study of the factors which limit the effectiveness of protection networks, and consideration of alternate approaches to achieve ESD hardness.

The limiting factors which are expected to determine the electrical overstress sensitivity

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of micron and submicron design rule microcircuit technologies were investigated using computer-aided modeling techniques. Network analysis codes were used to exercise lumped circuit analogs of the electrical and thermal properties of the devices under study when subjected to ESD stress. Simple time domain network analysis codes suitable for microcomputers were used and are discussed in the report. The minimum cross-sectional areas of aluminum and polysilicon interconnects and semiconductor devices which are capable of withstanding an ESD event were established.

Two candidate submicron technologies were considered in this study, CMOS and NMOS. Existing CMOS input protection networks were found to be effective. However, existing input protection networks for NMOS were found to suffer from high series resistance which limits the effectiveness of these networks.

An input protection network for NMOS based on conduction through avalanche injection is proposed. Avalanche injection offers a low impedance mode of conduction but is characterized by current controlled negative resistance which tends to constrict current. Characteristics of the submicron process offer the possibility of optimizing an avalanche injection device to achieve a simple and highly effective input protection network, and to control current constriction.

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EVALUATION

Advances in integrated circuit technologies are resulting in basic circuit structures which are increasingly sensitive to electrostatic discharge (ESD) damage because of decreasing oxide thicknesses, shallower junction depths and smaller junction areas. A comparison of the sensitivity of present day integrated circuits to damage by ESD to that of devices designed only a few years ago must be done on a vendor-to-vendor basis and often, unfortunately, within some vendors on a department or designer basis. Even so, certain vendors' product lines have exhibited reduced ESD sensitivity in spite of technology advances. These cases indicate that significant progress has been made in the design of effective ESD protection networks which are integrated into virtually all of today's devices.

Further progress must be made for two reasons: 1) future devices are expected to be more sensitive to damage as scaling continues and 2) the best protective networks available today cannot withstand a healthy zap from a human (>5000v, 100 pf, 1500 ohm test) or a low level zap from themselves (2000v, charged device test).

Many of the major semiconductor manufacturers have published the results of their own in-house design evaluations of new ESD protection networks. Several major users have published test and evaluation results on the ESD protection networks used on a wide cross-section of popular device types available today. Many practical lessons have been learned about protection network design and layout, but in the end, the networks which work best have not been fully understood in terms of the physics of their operation. This is so because the good protective network is small and conducts very high currents and these requirements push protection network current conduction mechanisms into the regime of second breakdown. This class of problems is only now yielding to the most sophisticated computer modelling and simulation efforts, and we believe that the use of these techniques to understand and design improved ESD protection networks has been limited.

The present work was undertaken as a small step toward the better understanding of factors which determine ESD sensitivity, the requirements which will be placed on future protection networks and finally, the design of superior ESD protection networks. The conclusion reached by this study is that the same technology advances which have made devices increasingly sensitive open new possibilities for designing very fast, low impedance, reasonably sized shunt elements. The challenge which remains is to invent, simulate and fabricate structures in which filamentary current constriction in second breakdown is not prevented but rather is controlled over the ranges of time and current required to survive an ESD event.

Daniel J. Burns

DANIEL J. BURNS
Project Engineer

SECTION I
INTRODUCTION

The objective of this program was to further define the electrical overstress (EOS) sensitivity characterization procedures for microelectronic devices and to investigate the EOS sensitivity of micron and submicron linewidth circuit structures. Another objective was to investigate improved EOS protection schemes and evaluate their benefits versus performance and cost penalties.

Four major tasks were identified as steps in meeting these objectives:

(1) Literature Search

(2) Definition of Test Procedure and Apparatus

(3) Investigation of Limiting Factors

(4) Investigation of Alternative Approaches

This report summarizes the work in all four tasks.

The goal of task 1 (Literature Search) was to identify the important parameters of the "Human Body" model and "Device Charge/Discharge" model applications and to identify specific test conditions, test procedures, and data analysis methods. Also, test methods for studying conductor line and junction burnout were identified. This information was used in defining the test procedures in task 2 (Definition of Test Procedure and Apparatus) and is presented in bibliographic form in appendix C.

The goal of task 2 was to define test procedures and apparatus appropriate to testing the EOS sensitivity of microelectronic devices. Since this program involved no original research into the phenomenology of EOS generation, the test procedure and apparatus definitions were based on the results of the literature search. Our evaluation indicated that the Human Body Electrostatic Discharge (ESD) event model recommended by the International Electrotechnical Commission is suitable for screening microelectronic devices. Thus, no new Human Body ESD model was proposed. Information on the Device Charge/Discharge ESD event was limited. The only model found in the literature was selected for these investigations and is presented in detail in section IV.

Task 3 (Investigation of Limiting Factors) was the heart of the program. An engineering approach was used rather than a detailed physics approach. The baseline ESD threats defined in task 2 were used. In order to establish the probable configuration of submicron devices, the scaling laws of microelectronics were examined and are reviewed in section II. Based on this study and information from the literature search, baseline process technologies for submicron devices were established and are presented in section III. Existing input protection networks were examined as a background for the study. The results of this examination are given in section V.

Circuit analysis codes were used to study limiting factors. The electrical response of the microelectronic structures was modeled directly in the codes, and the thermal response was modeled using electrical analogs for the thermal elements. The electrical and thermal models were coupled together so that effects such as temperature dependent resistivity could be properly modeled. Simplified circuit analysis codes suitable for use on a microcomputer were used in most cases, rather than more complex mainframe computer codes. These codes were appropriate to the level of detail required for the study and had the advantage of being inexpensive and easy to run. Sample versions of two codes used are presented in appendix B. Materials response data used in the modeling are presented in appendix A. The results of task 3 are presented in section VI, and the results of verifications against experimental data in section VII.

Several alternative approaches were investigated in task 4 (Investigation of Alternative Approaches). Since existing CMOS protection networks were found to be quite good, effort was directed at NMOS protection schemes. The NMOS process does not allow as many options for protection because it does not use isolated P+ diffusions. An improved NMOS protection network is presented in section VIII.

SECTION II
SCALING OF INTEGRATED CIRCUITS

Electronics is evolving toward miniaturization and its potential advantages of high speed, improved reliability, and lower weight, power dissipation, and cost. The incentive to reduce dimensions has continued at the integrated circuit level. The principle of scaling is one approach used to reduce the size of integrated circuits. Its basic objective is to preserve the original device characteristics in miniaturized geometry. In scaling, all dimensions of an integrated system, including those vertical to the surface, are divided by a constant scaling factor. This also applies to the supply voltage. Using this convention, all electric fields in the circuit will remain constant and many nonlinear factors affecting performance will not change as they would in more complex scaling.

Scaling will affect major system parameters. The transit time of carriers across a device, the gate capacitance, and drain-to-source current of each individual transistor will decrease. The switching power and dc power of each transistor will decrease by the square of the scaling factor, while the switching energy will decrease by the cube of the scaling factor. The power dissipated per unit area in the transistors, however, will remain constant.

Eventually, deviations must be made from scaling principles to build functional devices. As devices are reduced in dimensions, higher substrate doping is required to reduce the depletion regions of the drain and source to allow closer spacing. Increasing substrate doping requires a decrease in the drain voltage to avoid drain-substrate breakdown and drain-source punch-through. Reducing the drain voltage while increasing the substrate doping requires the oxide thickness to be reduced to a point where a low voltage can invert a highly doped substrate. Eventually, fundamental limitations of oxide tunneling and doping fluctuations will constrict the reduction process.

Much research has been devoted to the fundamental limitations of scaling MOS devices. A typical MOS transistor of minimum size is shown

in figure 1 (reference 2). This transistor has an oxide thickness of 140 angstroms. The maximum electric field which a 140-angstrom oxide can withstand is about 15 MV/cm (reference 3), which is about 21 volts. This transistor will be used as a baseline device for the design and analysis of input protection networks for submicron devices. Therefore, the protection network must be capable of withstanding a Human Body ESD event.

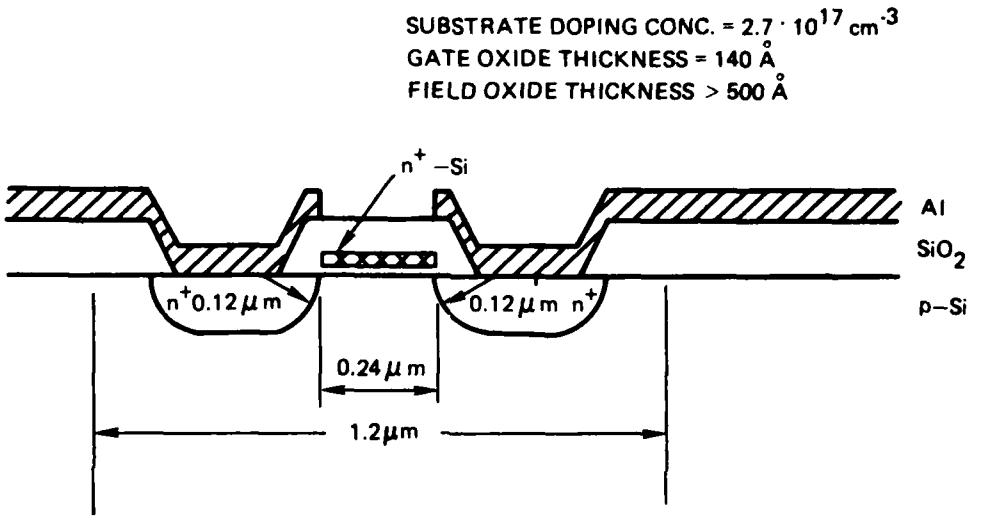


Figure 1. Typical Silicon Gate MOS Transistor of Minimum Size

While integrated circuit designers have focused their attention on developing functional submicron devices, the effect of external influences on device reliability has been neglected. One external influence which will affect reliability is electrostatic discharge. While devices are being scaled down in geometry, the ESD threat is as great as ever. An interconnect or junction which could normally handle an ESD current surge will now be required to handle a current density which is greater by the square of the scaling factor. An obvious solution is not to scale the input protection networks. Unfortunately, reproduction of existing input protection networks may be an inadequate solution. Since thinner gate oxides are required for submicron processes, the demands on the input protection network for attentuating

the ESD voltage will be more severe. Existing protection networks may have excessive capacitance for high speed gates manufactured using VLSI/ VHSIC technology. The aluminum and polysilicon interconnection films for a submicron process are likely to be thinner, resulting in behavioral changes in the network. Finally, input protection networks demand large areas which, if reduced, could result in significant savings.

SECTION III
TECHNOLOGY FOR SUBMICRON DEVICES

A. THE NMOS PROCESS

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the primary device used in VLSI circuits. ICs using MOSFETs were originally based on P-channel (PMOS) devices, however, N-channel (NMOS) devices, with their higher electron mobility, have dominated the IC market since the early 1970s.

Table 1 outlines a proposed submicron NMOS process (reference 4). Starting materials for the process are P-type wafers typically doped at $1x10^{15}$ atoms per cubic centimeter. The process begins by growing a 0.35-micron field oxide across the entire wafer. The entire surface is then implanted with high energy boron ions which penetrate the field oxide and increase the surface concentration to set the threshold voltage of the enhancement mode transistors and to form the channel stops. Cuts are now made in the oxide to define the regions where arsenic is to be implanted to form the depletion mode devices. After the arsenic ion implantation, the gate oxide is grown and polysilicon is deposited and etched to delineate the gates. The entire wafer is then exposed to arsenic ion bombardment to form the drain and source regions. The arsenic will be deposited through the gate oxide in those regions not protected by field oxide or polysilicon. Contact windows are then etched and aluminum is deposited and etched to form the metal interconnections. A cross section of the completed process, which will be used as a baseline for design purposes, is shown in figure 2.

B. THE CMOS PROCESS

Complementary Metal Oxide Semiconductor (CMOS) integrated circuit technology has emerged as one of the most important VLSI technologies. The major advantage of CMOS is low power consumption which becomes an

TABLE 1. WAFER PROCESS OUTLINE

(substrate is 6 to 8 Ω-cm, B doped)

1. Grow field oxide, 3500 A
2. Ion implant B, 150 keV, 2×10^{12} cm^{-2}
3. Active-area level lithography, (+) resist
4. Field oxide etch
5. Ion implant B, 150 keV, 0.5×10^{12} cm^{-2} (optional)
6. Depletion level lithography, (+) resist
7. Ion implant As, 60 keV, 3×10^{12} cm^{-2}
8. Grow gate oxide, 250 A
9. Deposit polysilicon, 1500 A
10. Polysilicon, level lithography, (+) resist
11. Etch polysilicon; etch oxides
12. Deposit polysilicon, 2000 A
13. Polysilicon level lithography, (-) resist
14. Etch polysilicon
15. Ion implant As, 30 keV, 7×10^{15} cm^{-2}
16. Grow thin oxide, deposit PSG, and planarize
17. Window-level lithography, (+) resist
18. Etch oxide
19. Form silicide
20. Deposit polysilicon plus Al
21. Metal level lithography, (-) resist
22. Etch Al, etch polysilicon
23. Sinter Al, metallize backside

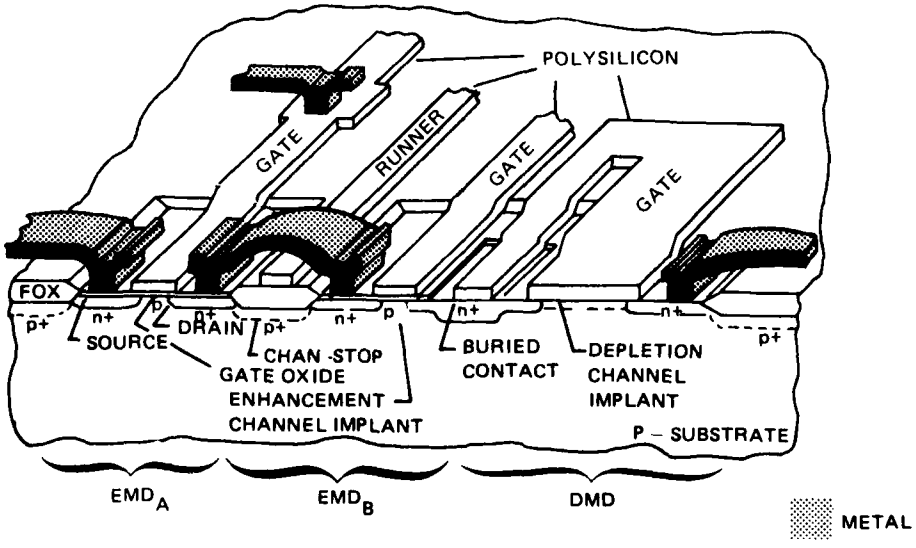


Figure 2. NMOS Structure

even greater advantage as integrated circuit density increases. As devices are scaled down, the power per unit area remains constant and, hence, heat removal requirements remain essentially constant. Power supply voltage often deviates from scaling principles for two reasons. First, because ICs must interface with a variety of other IC families designed to operate at a standard power supply voltage, pressure exists to operate the submicron circuitry at the standard voltages. Second, to be able to switch, the ratio of transistor on-to-off conductance must be much greater than unity; therefore, the voltage operating the circuit must be many times kT/q. For this reason, even those circuits optimized for operation at the lowest possible supply voltages still require a power supply voltage of at least 0.5 volts. When the power supply voltage can no longer be scaled with device dimensions, the power per unit area will increase creating the limiting factor of heat removal from the integrated circuit. Since CMOS consumes much less power than NMOS, it is not limited by heat removal. The lower power dissipation of CMOS also aids in preventing failures due to metal migration. The phenomenon of metal migration is a strong function of current density in metal interconnects.

The disadvantages of CMOS, with respect to NMOS, are greater processing complexity, larger area requirements per switching device, and greater input capacitance. However, modern CMOS processes have been simplified making NMOS and CMOS comparable in complexity.

A typical fabrication sequence for a CMOS integrated circuit is shown in figure 3. The typical starting material for the CMOS process is N-type material. A tub of P-type semiconductor is formed by implantation or diffusion. After the tubs are driven in, the source and drain regions of the P-channel transistors are implanted in the N-type regions. Subsequently, the source and drain regions of the N-channel transistors are implanted in the P-type tubs. Finally, a metalization step is used to form device interconnection.

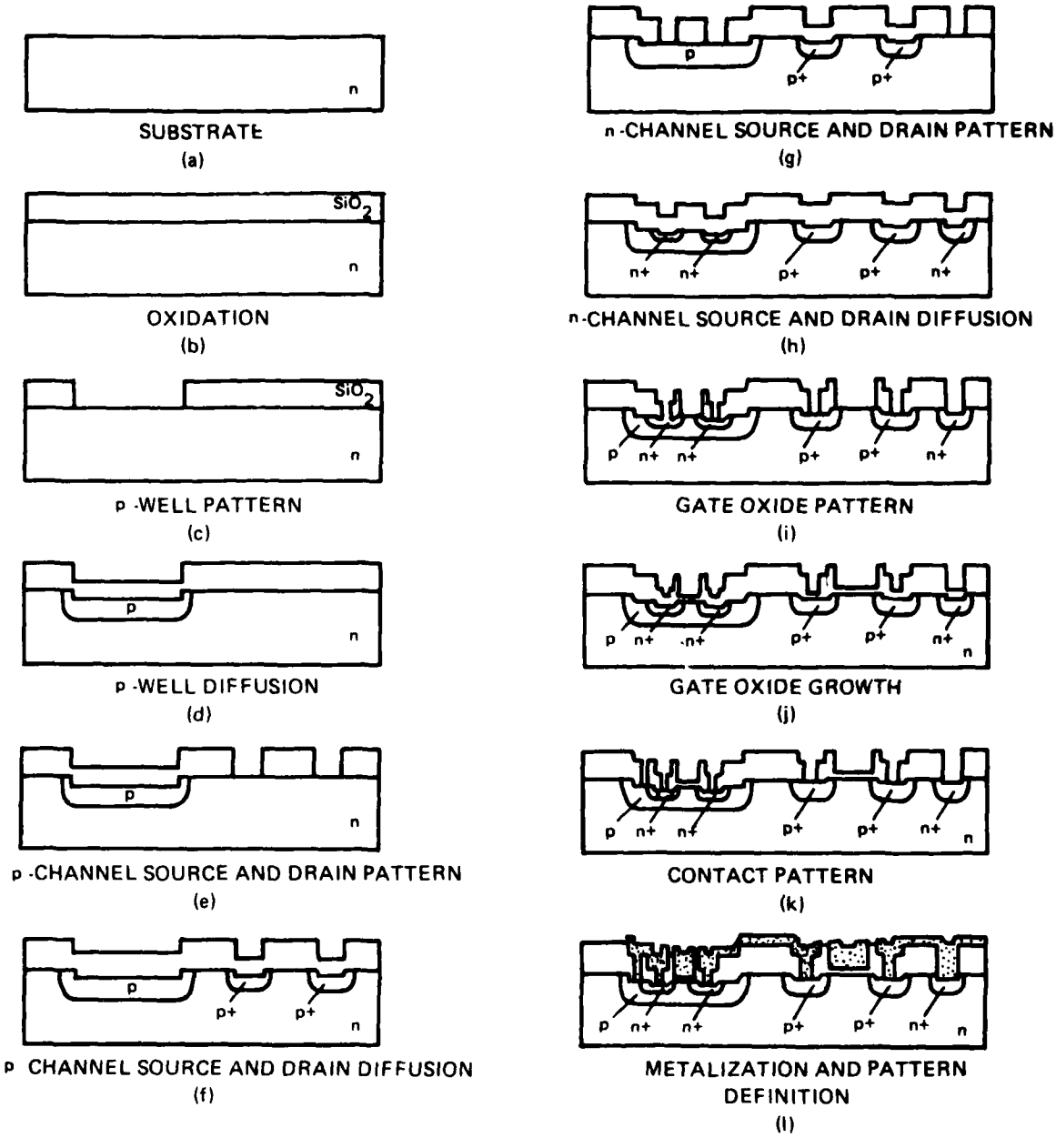


Figure 3. The CMOS Process

SECTION IV
ELECTROSTATIC DISCHARGE

A. HUMAN BODY ESD

Anyone who has received a mild shock after walking across a rug and touching a door has experienced a Human Body ESD event. Its basic mechanism is friction between two insulating materials of different dielectric constants. One material will give up electrons at the surface, while the other material will pick up electrons. This effect is called triboelectricity. For Human Body ESD, the two insulating materials are usually the soles of the shoes and a carpet. As a charge develops on the soles of the shoes, a compensating charge develops on the Human Body by the process of electrostatic induction across the insulating soles.

The electrostatic potential between the Human Body and ground is equal to the charge induced in the body divided by the Human Body capacitance. A typical induced charge is 0.6 microcoulombs, and a typical body capacitance is 150 pf which produces an electrostatic potential of 4 kV. However, electrostatic potentials of up to 20 kV are possible.

When a charged Human Body comes in contact with a grounded object, the discharge takes place in a few tens of nanoseconds accompanied by peak currents in the tens of amperes. Such a surge of high-voltage, high-current electricity represents a major threat to electronic components. The resultant damage can be divided into two categories, oxide rupture and burnout, although both failure mechanisms are thermal in nature.

Oxide rupture occurs when the dielectric strength of the silicon dioxide overlying a device is exceeded. Because of the nonlinear conduction properties of silicon dioxide, the current flow is unstable and concentrated into a very narrow region. The intense heating in this region may be sufficient to melt or vaporize the silicon dioxide, often resulting in a short between the interconnect and the silicon substrate. Since very little energy is required to destroy the oxide, oxide rupture can be considered a voltage-dependent phenomenon.

Device-or interconnect burnout requires a substantial amount of energy. A 150-pF Human Body capacitance charged to 4 kV contains 1.2 mJ of energy which is more than sufficient to cause thermal destruction of a small geometry device.

The literature search for the current program revealed considerable ongoing research on defining an appropriate Human Body model. A wide range of models and model parameters has been suggested for the Human Body ESD event depending on measurement techniques and conditions. Most of the models cited use a simple capacitor, modeling the Human Body capacitance, discharging through a resistor, representing the Human Body resistance, into the device under test. The values of the capacitors ranged from 100 pF to 500 pF and the values of the resistors ranged from 100 ohms to 5000 ohms. Some of the models allowed for multiple pulses or included features modeling the distributed nature of Human Body capacitance and resistance. Model voltages ranged from 1 kV to 25 kV.

In a previous program for RADC to develop specifications for microcircuit electrical overstress tolerance, BDM recommended a Human Body ESD model consisting of a 100-pF capacitor charged to a nominal 1 kV and discharged through a 1500-ohm resistor to the device under test. The test configuration is shown in figure 4. This model was based on the results of literature surveys conducted up to 1977.

The International Electrotechnical Commission (IEC) has recommended the model parameters shown in figure 5 as a suitable model for the Human Body ESD event (reference 1). Since this circuit was recommended by the IEC, it was chosen as the model for computer simulations of the Human Body ESD event. The voltage across the capacitor was set to 4 kV in response to the Statement of Work's design goal for a protective scheme which can withstand and prevent device damage from a 4-kV Human Body model discharge. The values of the capacitor and resistor represent the most severe models found in the literature, a worse case than those previously recommended by BDM.

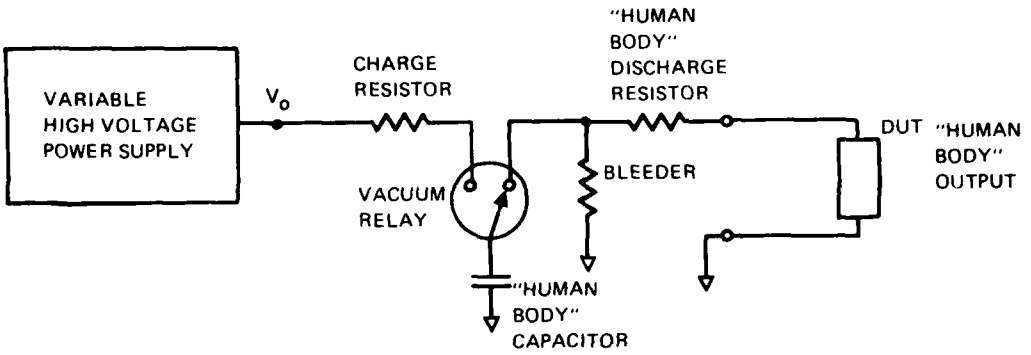


Figure 4. Human Body ESD Event Model

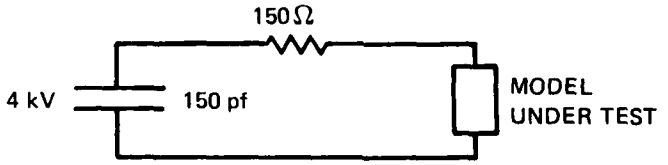


Figure 5. Simulation Model for Human Body ESD Event

B. DEVICE CHARGE-DISCHARGE EVENT

An ESD mode which has received less attention than the Human Body ESD event, but which may pose an equally serious problem, is the Device Charge-Discharge event. This event is basically the discharge to ground of a triboelectrically-charged device. A typical source of the triboelectric charge is friction between the device and its package (e.g., shipping tube) during handling. When the device is dumped out of its package onto a work surface, the charge will become manifested as an electrostatic potential. The magnitude of the electrostatic potential will depend on the charge on the device and its capacitance with respect to its surroundings. If the device comes in contact with a path to ground, the device will lose its charge in a very large surge of current.

The maximum charge that has been measured on an integrated circuit package under practical conditions is about 3 nC (reference 12). The electrostatic potential of the device is given by:

$$V=Q/C$$

and the potential energy of the device is:

$$E=0.5CV^2$$

Thus, the potential energy and electrostatic potential of the device will be at a maximum when the capacitance is at a minimum for a fixed charge. For a typical 16-pin DIP placed on a conductive work surface, the minimum capacitance configuration is obtained by standing the device on its corner pins. In this configuration, the capacitance is about 1.5 pF which corresponds to an electrostatic potential of 2 kV and a potential energy of 3 μJ.

While the Device Charge-Discharge event does not have nearly as much energy as the Human-Body Discharge event, its current surge is potentially greater because of the current limiting resistance of the Human Body. Because of the potentially lower source impedance of the Device

Charge-Discharge, the peak voltage reached in a device may exceed the peak voltage produced by a Human Body ESD event.

A practical test configuration for the Device Charge-Discharge mode is shown in figure 6. The device orientation with respect to the ground plane establishes the device capacitance. A high voltage power supply charges the device and a vacuum relay discharges the device through a resistor used to establish the resistance of the discharge path. An equivalent model suitable for computer analysis is shown in figure 7. Practical worst case values were chosen for the elements. The device is charged to 2 kV to represent 3 nC across a 1.5-pF device capacitance. The device is discharged through a 1-ohm resistor to the ground plane.

It is believed that this model represents a practical worst case based on current information. Other values of charging voltage or device capacitance may be appropriate in some cases.

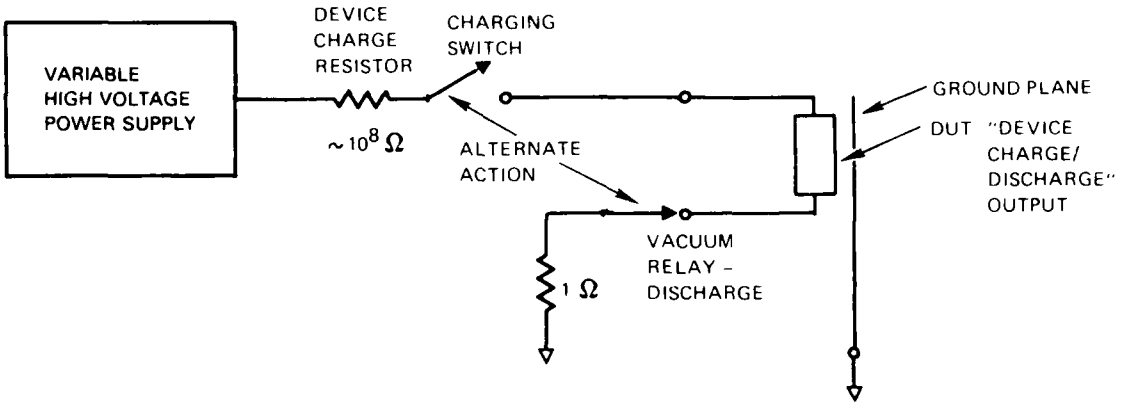


Figure 6. Charge-Discharge ESD Model

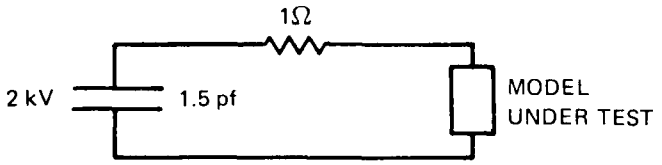


Figure 7. Simulation Model for Device Charge-Discharge

SECTION V

REVIEW OF EXISTING INPUT PROTECTION NETWORKS

A. CLAMP DIODE PROTECTION NETWORKS

The clamp diode input protection network shown in figure 8 is popular and effective for CMOS devices. Any transient which exceeds VDD or is less than ground potential will forward bias one of the diodes adjacent to the protected node. Forward biased diodes have the advantage of offering excellent low impedance current paths. During normal operation, the diodes are reverse biased. A resistor is usually added in series with the gate protection to limit the peak current. If the resistor is diffused, further input protection is offered by the forward conduction and reverse breakdown characteristic of the resistor.

The disadvantage of series resistance is the large voltage drop across the resistor which will appear for any appreciable value of resistance. The induced voltage may be sufficient to destroy the field oxide or induce current mode instability and destruction at the input of a diffused resistor. Polysilicon resistors are relatively sensitive to failure by thermal destruction (reference 14).

It has been reported that for large values of input resistance, the oxide may avalanche without destruction (reference 15). An input protection network based on this phenomenom might warrant further investigation.

The clamp diode input protection network is utilized by Texas Instruments (TI) for its High-Speed CMOS logic family. The TI input protection network, shown in figure 9, is advertised as offering input protection to an ESD of 4500 volts. The major difference between the TI input protection network and the CMOS protection network shown in figure 8 is that the VSS and VDD clamping diodes are directly in parallel and not separated by a series resistor. This approach results in a lower impedance ESD current path to ground.

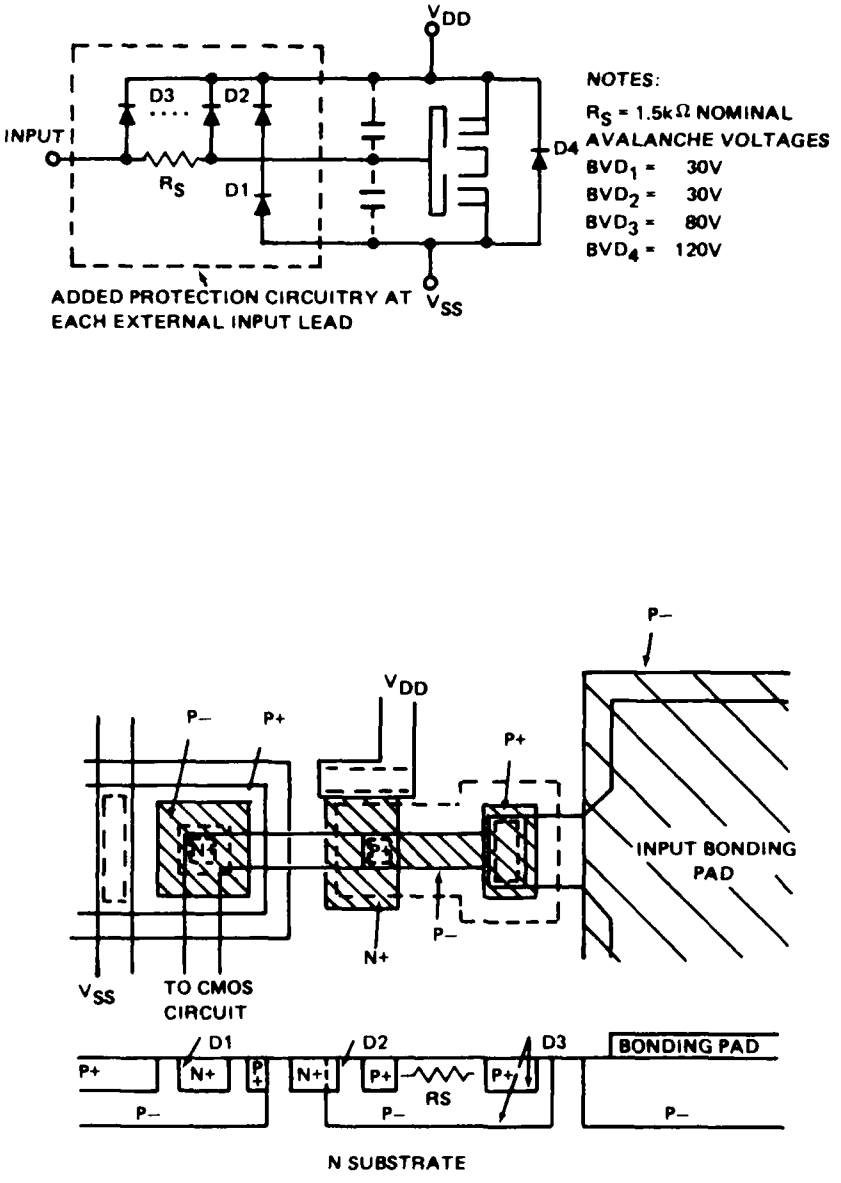


Figure 8. Clamp Diode Input Protection

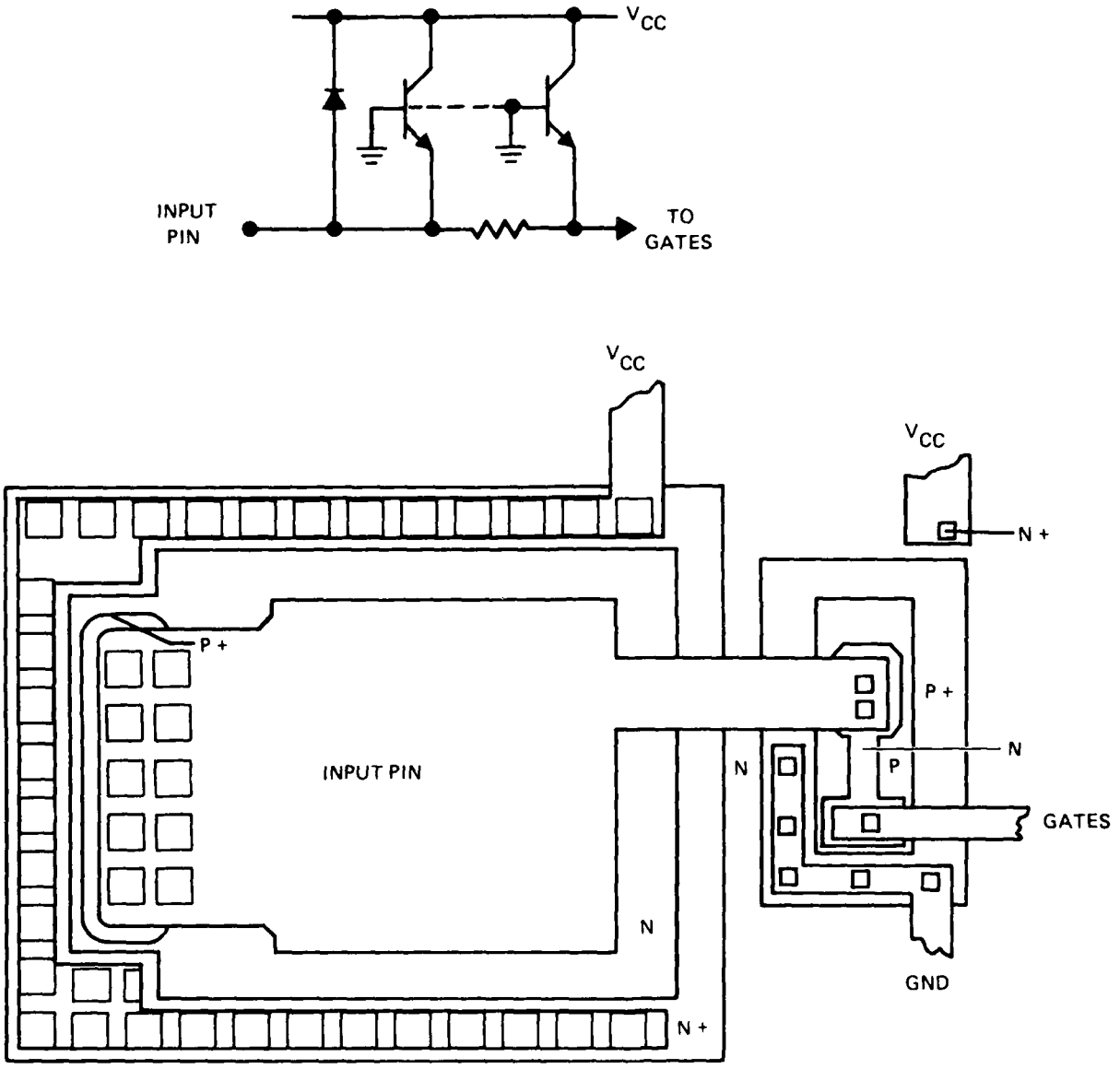


Figure 9. Protection Network Used by Texas Instruments for its High-Speed CMOS Logic Family

A disadvantage of clamp diode protection is that it cannot be readily fabricated on all VLSI and VHSIC candidate technologies. The clamp diode structure requires a P-diffusion which is isolated from ground. Isolated P-diffusions do exist as part of the CMOS process, but do not exist in the standard NMOS process.

B. ZENER DIODE

A common method of protecting the inputs of NMOS technology integrated circuits is to place use a diode between the input to be protected and ground or the substrate. If the transient input voltage exceeds the maximum input voltage, the diode will clamp the input voltage through avalanche conduction. If the transient input voltage goes negative, the diode will conduct in the forward direction. A major design problem for breakdown diode input protection networks is tailoring the breakdown voltage to a practical value. The breakdown voltage for a planar junction, illustrated in figure 10(a), is approximately (reference 7):

$$Vbd = 2.72 \times 10^{12} N^{-2/3}$$

For the baseline NMOS process of table 1, which uses a 6 ohm-cm substrate, the doping concentration would be 2×10^{15} and the corresponding breakdown voltage would be 170 volts. Curvature of the junction will intensify the electric field in the curved regions resulting in a somewhat lowered breakdown voltage as illustrated in figure 10(b).

One method of adjusting breakdown voltage is to place a grounded fieldplate over the edge of the P-N junction. The presence of the field plate increases the electric field in the depletion region at the surface as illustrated by figure 10(c). Unfortunately because only the junction at the surface is affected, the series resistance of the protection network is relatively high.

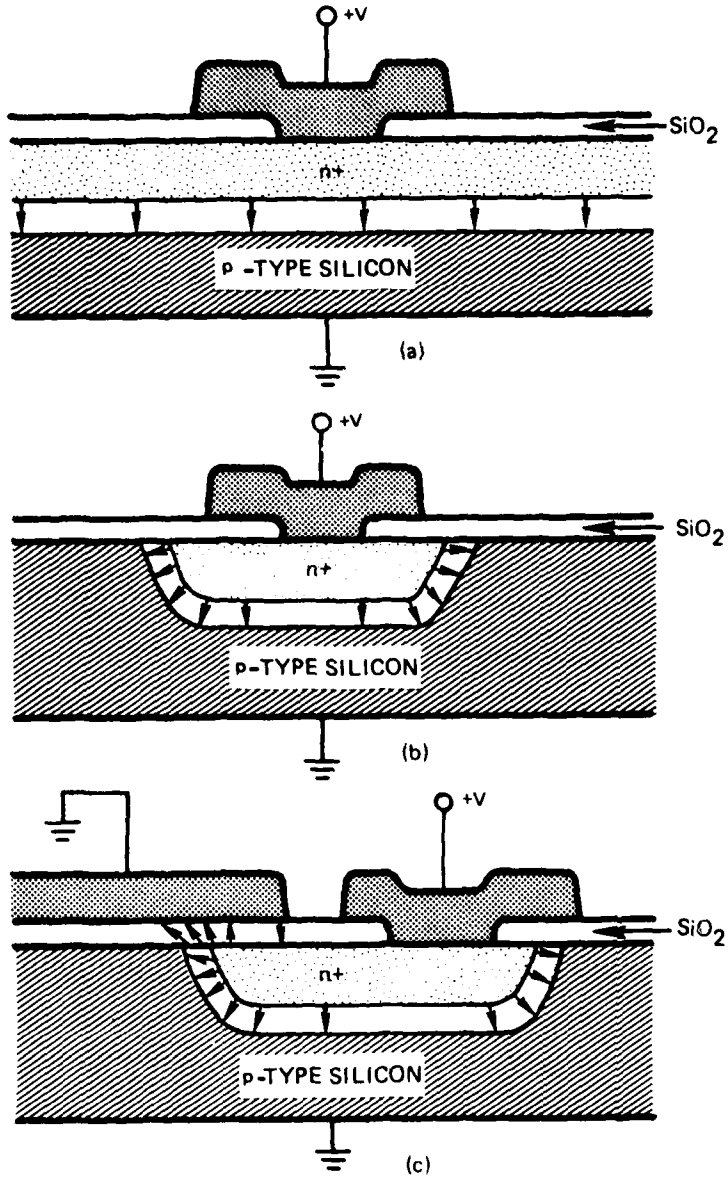


Figure 10. Zener Diode Protection Structures

A limiting factor in the ability of a zener diode to protect a gate from destruction is a parasitic resistance. One component of parasitic resistance is the bulk resistance offered by the high-resistivity substrate which may be approximated by (reference 11):

$$Rs = \frac{\rho}{2d}$$

For the baseline NMOS starting substrate resistivity of 6 ohm-cm a diode with a 100-micron diameter will have a spreading bulk spreading resistance of about 300 ohms which is unacceptably large.

Another component of parasitic resistance is space-charge resistance given by:

$$R = \frac{W_d^{\,2}}{2\varepsilon_s V_{SL} A}$$

The space-charge resistance can easily be high enough to render the protective structure useless against ESD. For example, if the doping near the surface is about $1x10^{17}$, the breakdown voltage will be about 10 volts and the depletion region width about 0.4 microns. Assuming a device length of 100 microns and a junction depth of 1 micron, the space-charge resistance will be about 75 ohms. For an ESD surge current of 20 amperes, the voltage drop will be 1.5 kV.

Another method of reducing breakdown voltage is the reach-through diode structure. Reach-through occurs in P+N-N+ or N+P-P+ structures when the depletion region spreads through the entire width of the lightly doped region as shown in figure 11(a). When the depletion region reaches the highly doped volume, it is effectively stopped, even though the reverse bias voltage may be increasing. This causes the electric field across the depletion region to increase faster and breakdown to occur earlier than in a P+N- or P-N+ diode. Investigators (reference 5) have suggested the use of a P- on P+ epitaxial structure, shown in figure 11(b), to construct large area reach-through diodes.

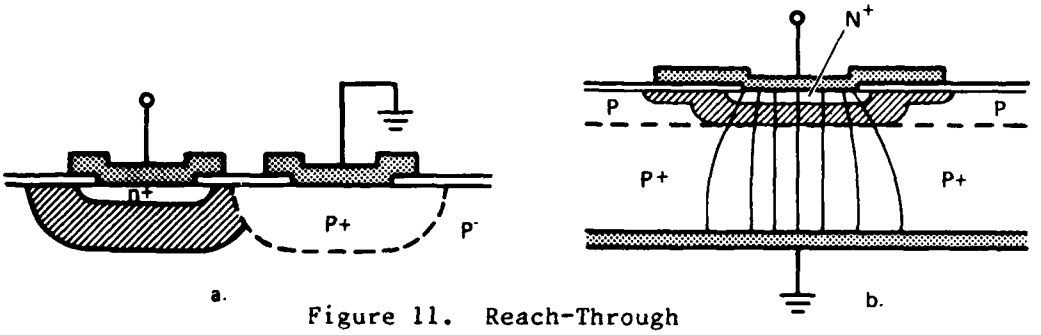


Figure 11. Reach-Through

The space-charge resistance of a reach-through diode fabricated using epitaxy for large surface areas may still be appreciable. Assuming a practical epitaxial layer thickness of 1 micron, the space-charge resistance of a square diode 100 microns on the side (about the size of a bonding pad) is about 4.7 ohms. The peak Human Body ESD model current is about 26 amperes which will induce 122 volts across the diode and exceed the baseline protection requirements.

C. PUNCH-THROUGH

Punch-through occurs in N+P-N+ or P+N-P+ structures. When the depletion region spreads across the lightly doped region, the opposing heavily doped regions are effectively connected together and current may flow through the device as shown in figure 12(a).

Conduction in a punch-through structure is space-charge limited, therefore, there is a space-charge resistance associated with the structure. The resistance for the thin oxide transistor structure is often prohibitively high. For example, in a structure consisting of 1 micron deep N+ diffusions 100 microns long, separated by a gap 1 micron wide, the space-charge resistance will be 472 ohms. Investigators (reference 5) have bypassed this difficulty by proposing a P-N+ expitaxial structure shown in figure 12(b) as a low impedance alternative.

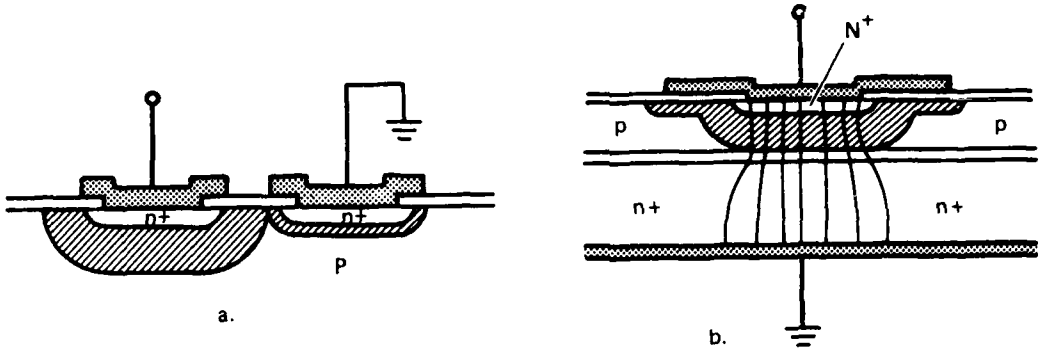


Figure 12. Punch-Through

D. PARASITIC TRANSISTOR

Parasitic NPN transistor action can occur between closely spaced N+ diffusions before punch-through. If avalanching of the biased junction occurs, as shown in figure 13, the avalanche current can induce a voltage across the bulk resistivity of the P-material which will forward bias the grounded N+ diffusion causing electrons to be injected into the "collector." The injected electrons will undergo multiplication when they pass through the avalanche region which will increase electron injection. The resulting regenerative process will result in a "breakover" characteristic. The injected electrons will reduce the space charge of the avalanching junction resulting in a very low dynamic impedance once switching has occurred as illustrated in the actual NMOS I-V characteristic of figure 14 (reference 9).

E. MOS TRANSISTOR

A positive overstress voltage may be applied to a gate of an N-channel MOS transistor to turn on the transistor which will shunt the overstress voltage to ground or the power supply. The thick oxide transistor structure uses positive overvoltage transients to turn on an NMOS transistor which has been fabricated using field oxide instead of gate

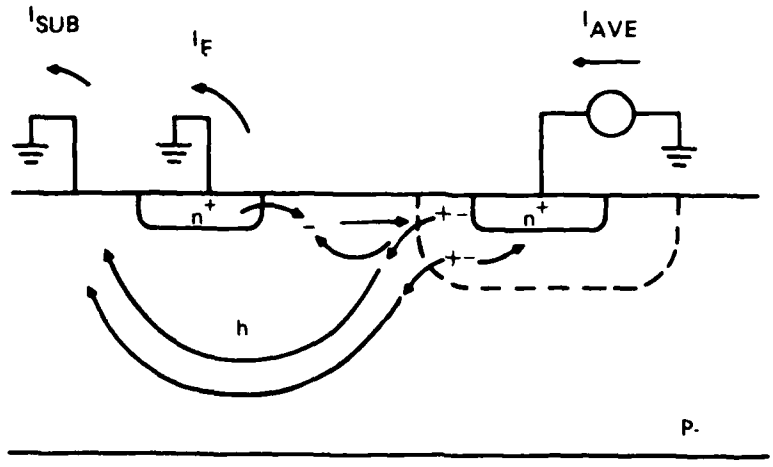


Figure 13. Parasitic Transistor Instability

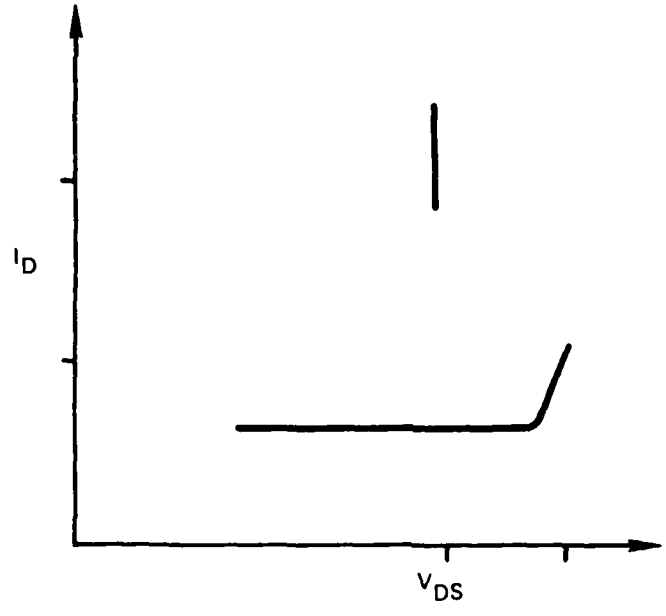


Figure 14. I-V Characteristic of Parasitic Transistor Protective Network

oxide. When activated, the thick oxide transistor will allow the transient to flow to ground through the conducting channel of the transistor. An advantage of using thick oxide is that the protection network is not as threatened by overvoltage transients as schemes which use thin oxides.

The contribution of the channel conduction term can be estimated by assuming a thick-oxide transistor (3500 angstroms) where the charge carriers are moving at scattering limited velocity. The charge density induced in the channel may be expressed as:

$$Q = \frac{-\varepsilon_s WL(Vgs-Vt)}{Tox}$$

The drain current is found by dividing the charge density by the transit time or:

$$Ids = \frac{-\varepsilon_s LV_{SL}(Vgs-Vt)}{Tox}$$

For a device 10 volts above threshold and L is 100 microns, the drain current is only about 30 mA.

Since channel conductance is relatively low, it is probably not the dominant mode of current conduction under ESD stress and the advantages of a thick oxide transistor for ESD protection are questionable.

F. SPARK GAP

Spark gaps are merely two closely spaced serrated metal pads. Spark gaps are usually used in conjunction with other input protection schemes because of their high arcing voltages (300-400 volts). The use of spark gaps often conflicts with integrated circuit fabrication procedures, since many processes call for some type of conformal coating to protect the integrated circuit from moisture and debris.

SECTION VI
INVESTIGATION INTO LIMITING FACTORS

A. APPROACH

The limiting factors expected to determine the electrical overstress sensitivity of micron and submicron design rule microcircuit technologies were investigated through the use of computer-aided modeling and supported by an analytical effort. The principal use of computer-aided modeling was the simulation of the electrical and thermal behavior of electronic structures under electrical overstress. With the aid of the computer, complex geometries and nonlinear behavior, which are difficult to treat analytically, were studied.

The models utilized for computer analysis modeled the electrical and thermal behavior using analogous discrete electrical elements lumped into a network. The physical basis for using thermal analogs is discussed in Appendix D. The advantage of using these elements is that the resulting network is in a form suitable for analysis by existing circuit simulation codes such as SPICE. An example of an electrical analog for an electrothermal problem is shown in figure 15. This model, for an electrostatic discharge into a resistor, consists of an interlinked electrical portion and thermal portion. The electrical portion models the discharge of the Human Body capacitance through the Human Body resistance and through the resistor under test. The thermal portion consists of a current source, capacitor, and resistor. The current source is analogous to power and is set equal to the power being dissipated in the resistor which models the electrical behavior of the resistor under test. The capacitor models the specific heat of the device and will determine how fast the temperature rises for a given power dissipation. The resistor models heat loss to the surrounding environment, such as the air, and through the leads of the device. The voltage across the parallel thermal analog is proportional to the temperature of the device. Once the model is defined and executed using a circuit analysis computer code, the instantaneous temperature behavior of the resistor during and after the ESD can be monitored by the analyst.

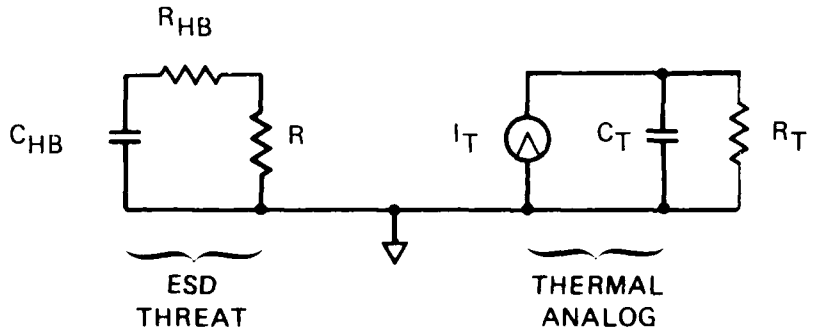


Figure 15. Modeling the Electrical Overstress Behavior of a Resistor

B. THERMAL MODEL DEVELOPMENT

The basic approach to developing a thermal model for an electronic structure is to divide the structure into finite volume elements. The number of volume elements chosen will be a trade-off between simulation accuracy and computational resources. The general philosophy utilized for this program was to choose the minimum number of volume elements necessary to achieve an acceptable simulation.

Each volume has an associated thermal capacity, modeled by a capacitor, and a thermal resistivity, modeled by one resistor for each face of the volume. The complexity of each volume element could be reduced if the geometry of the problem was such that heat flow was along fewer than three axes. The volume element in three dimensions is shown in figure 16(a).

If heat flows along only two axes (e.g., in a thin film on a thermally insulated substrate), the volume model is reduced to that shown in figure 16(b). If the heat is constrained to flow along only one axis, (e.g., from a planar source), the model is reduced to that shown in figure 16(c). And if the material is heated uniformly or quickly so that significant heat does not flow, a single capacitor, shown in figure 16(d), will suffice.

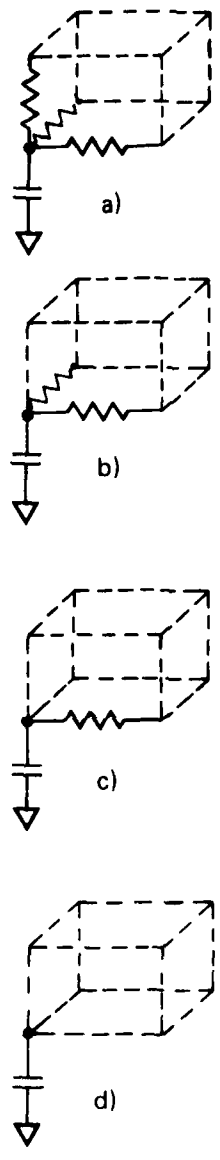


Figure 16. Electrical Analog of Heat Flow and Storage

The value of the capacitor which models the specific heat of the finite volume is:

$$C = SV$$

Where S is the specific heat of the material and V is the element volume.

The specific heats of silicon, aluminum, and silicon dioxide as a function of temperature are given as plots in appendix A. For purposes of modeling, specific heat was assumed to be constant with temperature. The chosen values of specific heat of some typical electronic materials expressed in units of watt-seconds per cubic centimeter per degree Kelvin are listed in table 2.

The values of the resistors which model heat flow were determined from thermal conductivity data. The behavior of thermal conductivity as a function of temperature for silicon, aluminum, and silicon dioxide are given as plots in appendix A. The thermal conductivity of aluminum was assumed to be constant as a function of temperature, but the thermal conductivity of silicon varies strongly with temperature and was modeled as a function of temperature. The values and functions of thermal resistivity of some common electronic materials chosen for modeling purposes are given in table 2 expressed in units of centimeters-degrees Kelvin per watt.

The electrical resistance analog of the thermal resistance from face-to-face of a volume element is found from:

$$R = PW/A$$

Where P is the thermal resistivity, W is the distance between opposing faces, and A is the area of a face.

C. ELECTRICAL MODEL DEVELOPMENT

1. Bulk Properties

The electrical behavior of bulk material was modeled by dividing the material into incremental volumes. The number of volumes

TABLE 2. IMPORTANT PROPERTIES OF MATERIALS

ALUMINUM	
MELTING POINT	$934^{o}K$
SPECIFIC HEAT	2.43 Watt-sec/cm^3 ^{o}K
THERMAL RESISTIVITY	0.421 cm ^{o}K/watt
ELECTRICAL RESISTIVITY	2.65×10^{-6} ohm-cm
COEFFICIENT OF RESISTANCE	$0.00429/^{o}K$
SILICON	
MELTING POINT	1683 ^{o}K
SPECIFIC HEAT	1.65 watt-sec/cm^3 ^{o}K
THERMAL RESISTIVITY	T/336 cm ^{o}K/watt
POLY-SI COEFFICIENT OF RESISTANCE	$1 \times 10^{-3}/^{o}K$
SILICON DIOXIDE	
MELTING POINT	>1600 ^{o}K
SPECIFIC HEAT	2.27 watt-sec/cm^3 ^{o}K
THERMAL RESISTIVITY	71.4 cm ^{o}K/watt
SAPPHIRE	
SPECIFIC HEAT	3.3 watt-sec/cm^3 ^{o}K
THERMAL RESISTIVITY	4.45 cm ^{o}K/watt

chosen is a trade-off between simulation accuracy and simulation time. The electrical behavior of each volume element can be modeled by one or more resistors. The number of resistors required to model a volume element is a function of the device geometry. If current can flow in three dimensions, three resistors per volume element are required.

The value of the resistors for each volume element are calculated as:

$$R = \rho W/A$$

Where ρ is the bulk resistivity of the material, W is the distance between opposing faces of the volume, and A is the area of a volume face.

In general, the electrical volume elements will have a one-to-one correspondance with the thermal volume elements. The two will then be linked. The values of the electrical resistance elements may be a function of the temperature of their thermal volume element, and the value of the current source which drives the thermal volumes will be a function of power dissipated in the electrical resistance elements. If the device is uniformly heated, only one thermal and electrical volume element is required for an adequate simulation.

a. Aluminum

Aluminum is commonly used in integrated circuit manufacture as a means of electrically interconnecting devices on the surface of the IC. A typical aluminum film is 1 micron thick. The resistivity of aluminum as a function of temperature is shown as a plot in appendix A. The resistivity of aluminum is a strong function of temperature which must be modeled to achieve reasonable simulation accuracy. The room temperature resistivity and temperature coefficient of resistance of aluminum are given in table 2.

b. Polysilicon

Polysilicon is used as gate electrodes for MOS devices, interconnections, and resistors. When used as an interconnecting medium, polysilicon is usually heavily doped to minimize resistance. Polysilicon

has a positive coefficient of resistance with temperature which is a characteristic of a metal rather than a semiconductor. Therefore, the same techniques used to investigate aluminum interconnects were used to investigate polysilicon interconnects. Heavily doped polysilicon usually has a resistivity between 0.001 and 0.01 ohm-centimeters. A typical polysilicon film has a thickness of 0.5 microns.

c. Silicon

The resistivity of silicon is a function of the number of charge carriers per unit volume and the mobility of the carriers. Carrier mobility is a function of temperature, doping, and the electric field. The number of carriers is a function of doping and temperature.

Mobility as a function of the electric field is essentially constant until the carriers reach a saturated velocity, V_{SL}, which occurs at an electric field, E_{sat}. The electric field at which velocity saturation occurs is about 1×10^4 V/cm. The scattering limited velocity is a strong function of temperature as illustrated in figure 17.

The resistivity of bulk semiconductors in low electric fields may be described as:

$$\rho = \frac{1}{qu_n n + qu_p p}$$

For N-type material:

$$n_n = \frac{1}{2}\left[N_D + \sqrt{N_D^2 + 4\, n_i^2}\right]$$

$$P_n = \frac{n_i^2}{n_n}$$

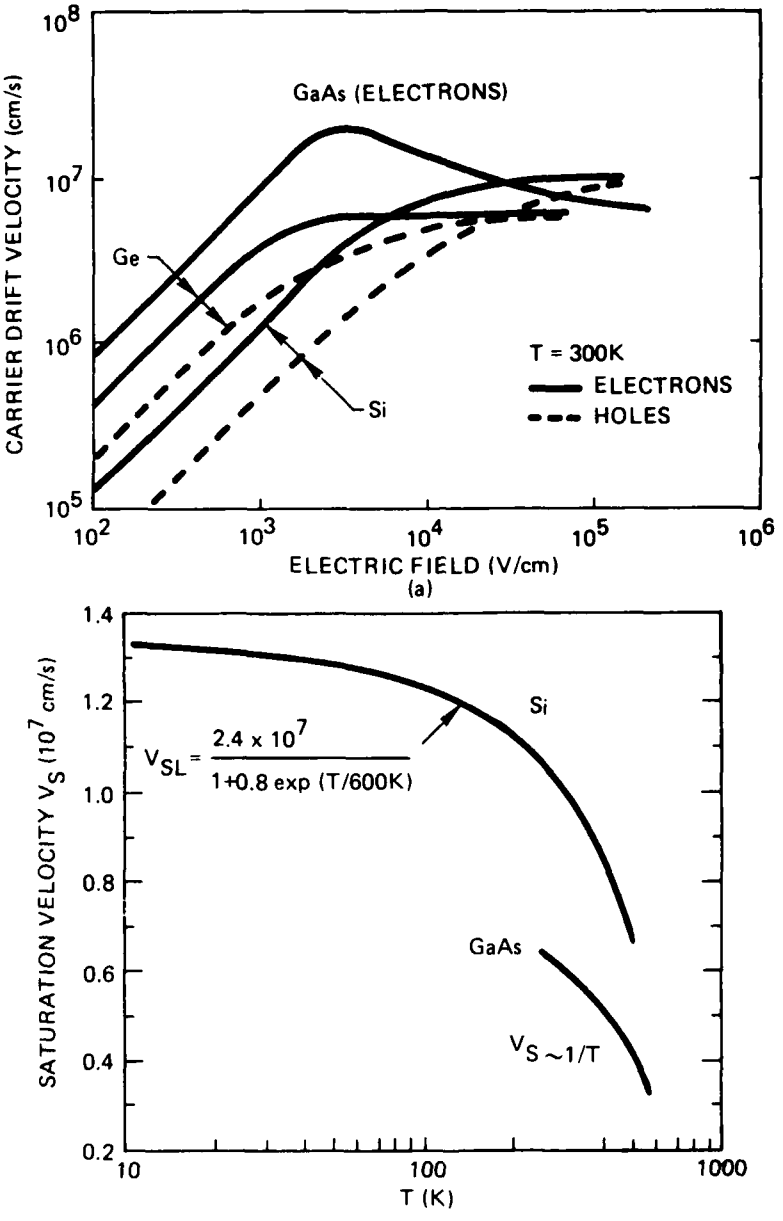


Figure 17. Carrier Behavior in High Electric Fields

For P-type material:

$$P_p = \frac{1}{2}\left[N_A + \sqrt{N_A^2 + 4\, n_i^2}\right]$$

$$n_p = \frac{n_i^2}{P_p}$$

Empirical expressions for mobility and intrinsic carrier concentrations as a function of temperature are:

$$n_i^2 = 15 \times 10^{32}\, T^3 e^{-1.21/kT}$$
$$u_n = 2.1 \times 10^9\, T^{-2.5}$$
$$u_p = 2.3 \times 10^9\, T^{-2.7}$$

These equations were implemented on an HP-85 with results given in figures 18 and 19. The results may be understood as follows: at low temperatures, the density of charge carriers is nearly equal to the doping density, but mobility is decreasing with temperature due to carrier interaction with thermal phonons. At high temperatures, the sheer number of thermally generated carriers begins to lower resistivity.

At low temperatures the resistivity of silicon has a positive coefficient with temperature. This characteristic will tend to spread current uniformly through the material. Eventually, a temperature will be reached where the resistivity will have a negative coefficient with temperature and thermal runaway is a possibility. The "turn-around" temperature has often been cited as a failure mechanism, but this is not always the case. First, resistivity is only meaningful in the low field region where mobility is essentially constant. Second, current constriction results from a true negative resistance and not necessarily from a negative temperature coefficient.

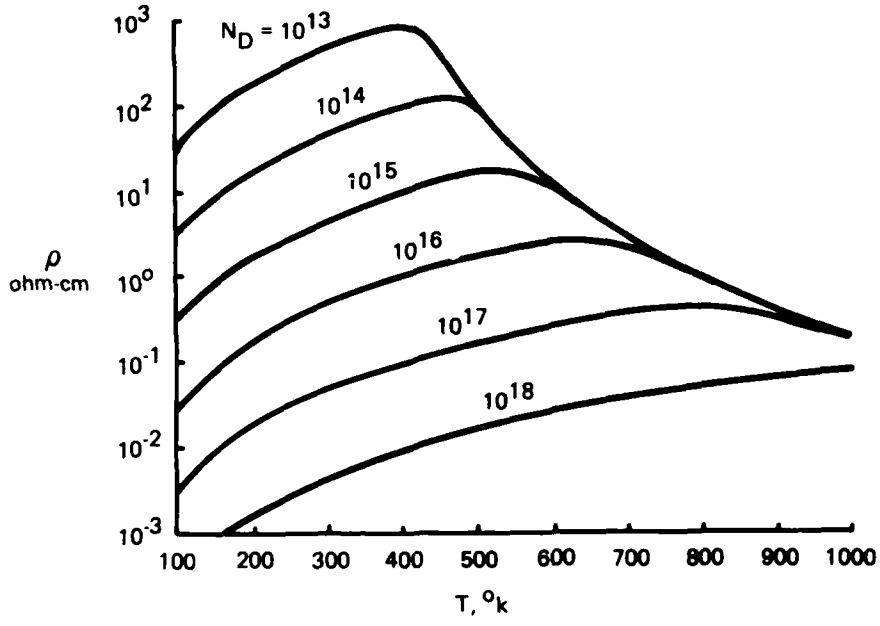


Figure 18. N-Type Resistivity as a Function of Temperature

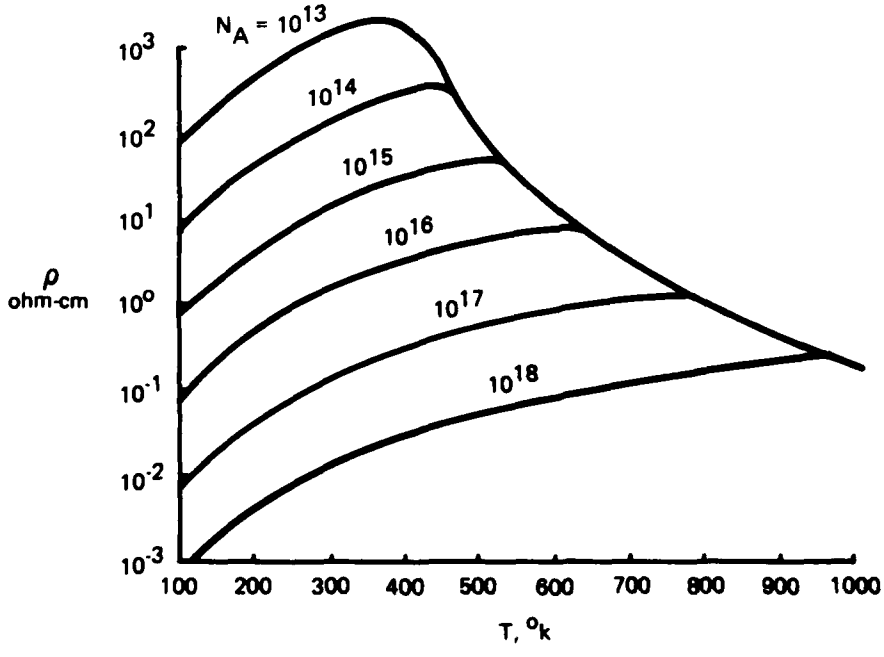


Figure 19. P-Type Resistivity as a Function of Temperature

The behavior of the bulk resitivity of silicon at high fields may be understood by considering the electrical behavior of a bar of N-type silicon shown in figure 20 (reference 13).

A bias across the bar will cause electrons to be injected at the cathode and holes to be injected at the anode. Because the bar is "long" the transit time of holes is much greater than the hole lifetime. Thus, holes are not able to traverse the bar and do not contribute to charge conduction. Therefore, injection is essentially due to a single carrier type (single injection). Single injection is characterized as a stable mode of conduction (i.e., positive resistance).

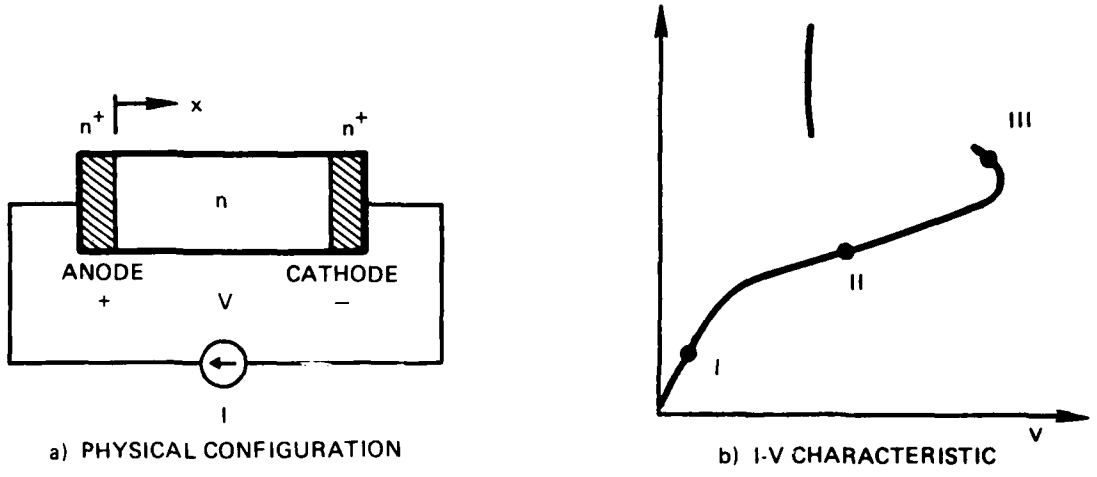
For low values of current, the bar behaves like a resistor (region I on the current-voltage characteristic plot of figure 20). The resistivity of the semiconductor in this region may be described by the curves of figure 18.

As current is increased through the bar, the velocity of the carriers will increase to carry the current. Eventually, the carriers will reach a scattering limited velocity which occurs when the electric field exceeds $1x10^4$ volts/cm. Scattering limited velocity is highly temperature dependent as illustrated in figure 17. The current at which scattering limited velocity occurs is:

$$I = AqV_{SL}N$$

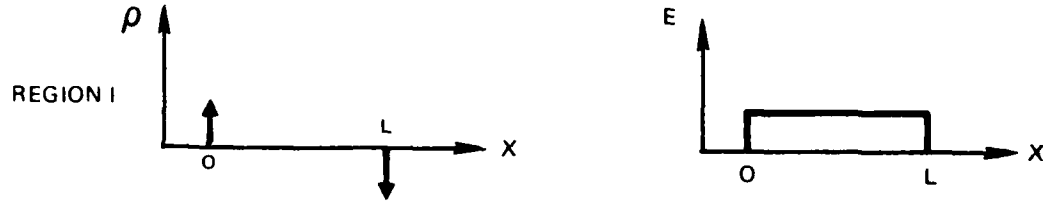
Where A is the cross-sectional area of the bar, q is the electronic charge, V_{SL} is the scattering limited velocity, and N is the background doping concentration.

If current increases further, the density of electrons injected into the bar must exceed the background doping concentration if the current is to be carried by charge carriers moving at scattering limited velocity. When the charge density exceeds the background doping density, charge neutrality is violated and the excess carriers will produce a space charge in the bar. Conduction is now space charge limited (region II in figure 20).

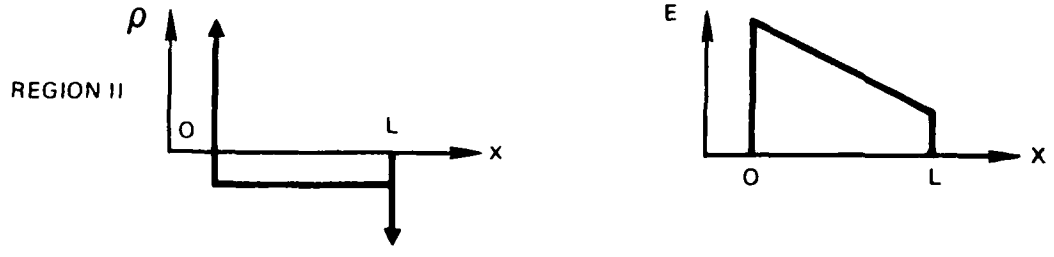


a) PHYSICAL CONFIGURATION

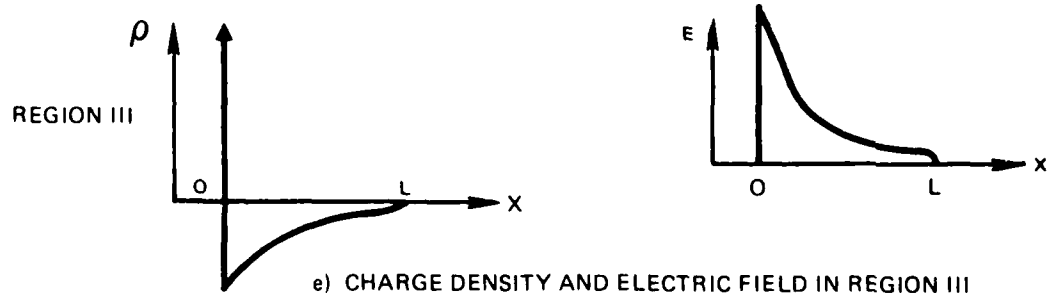
b) I-V CHARACTERISTIC



c) CHARGE DENSITY AND ELECTRIC FIELD IN REGION I



d) CHARGE DENSITY AND EI ECTRIC FIELD IN REGION II



e) CHARGE DENSITY AND ELECTRIC FIELD IN REGION III

Figure 20. The Behavior of Bulk Semiconductors under High Stress

The disturbance in the electric field due to the space charge is:

$$\Delta E(x) = \frac{Ix}{A\varepsilon_s V_{SL}}$$

Therefore, the peak electric field can be computed as:

$$E_{max} = \frac{IL}{A\ \varepsilon_s\ V_{SL}} + 1 \times 10^4 \text{ v/cm}$$

where the 1×10^4 v/cm term is the constant of integration and is the electric field at the onset of space charge limited conduction. The voltage across the device is found by integrating the electric field across the length of the device with the result:

$$V = \frac{IL^2}{2A\ \varepsilon_s\ V_{SL}} + (1 \times 10^4)\ L$$

The space-charge resistance is found by differentiating the voltage with respect to current to yield:

$$R_{SC} = \frac{L^2}{2A\ \varepsilon_s\ V_{SL}}$$

If the current is increased further, a point will eventually be reached where current flow becomes unstable (region III of figure 20). Instability results when conduction changes from single injection to double injection. Double injection can occur if the bar is short enough so that holes may begin reaching the cathode or through avalanche injection.

Avalanche injection, illustrated in figure 21, will occur when the peak electric field in the bar exceeds the critical value for impact ionization. When this occurs, hole-electron pairs will be produced. The electrons will quickly be swept out of the anode where the peak field lies, but holes will travel down the bar toward the cathode. The sudden influx of holes will act to cancel the space charge produced by the excess electrons in the central portion of the bar which will cause the space-charge region to become flooded with carriers. This redistributes the voltage drop along the bar as shown in figure 21a and b and results in higher fields near the anode which then forces the avalanching region to one end of the bar. The space-charge region will now take on the characteristics of a low resistance semiconductor. Current will now take the path with low space-charge resistance (where the highest density of carriers already exists) resulting in a regenerative current instability.

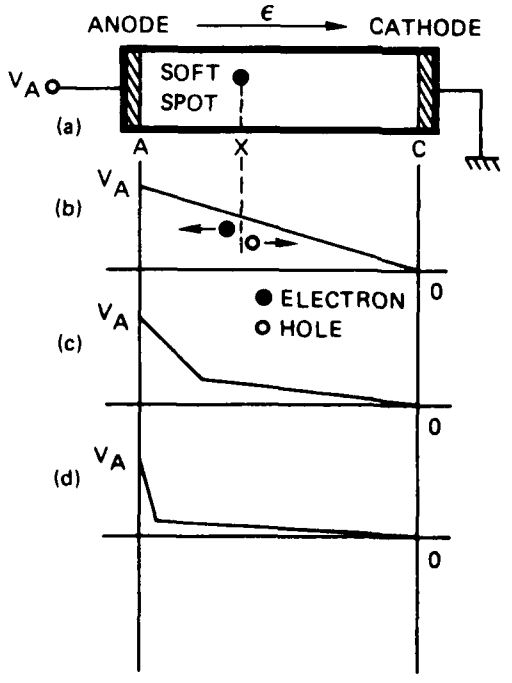


Figure 21. Avalance Injection

The diode will now have a bulk negative resistance, and the current will constrict into narrow filaments, called microplasmas since they consist of quasi-neutral regions, approximately 1 to 10 microns in diameter. Initially, the rate of hole-electron pair production in a microplasma is equal to the rate of loss of carriers by diffusion. An increase in pair production by raising the device voltage will be balanced by an increase in diffusion which is manifested as an increase in the diameter of the filament. Thus, the microplasma is inherently stable as long as the temperature remains below the point where thermally generated hole-electron pairs are significant. When the temperature rises to the point where thermally generated holes and electrons are an important component of the total current, thermal runaway will occur and a giant, or mesoplasma, will form. A typical mesoplasma can be observed as a glowing red spot 25 microns to 75 microns in diameter. Mesoplasmas have been associated with second breakdown and device destruction through melting.

Another method of inducing a mesoplasma is to heat a reverse biased junction to a high temperature. Thermal runaway can then occur if the device is heated to the point where bulk resistance takes on a negative coefficient with temperature, as indicated in figures 18 and 19 or if minority carrier leakage across the junction becomes significant. Both effects occur near the intrinsic temperature which is the temperature where the intrinsic carrier concentration becomes equal to the background doping concentration. The intrinsic temperature also marks the boundary between a stable microplasma and an unstable mesoplasma. A plot of the intrinsic temperature as a function of doping is given in figure 22.

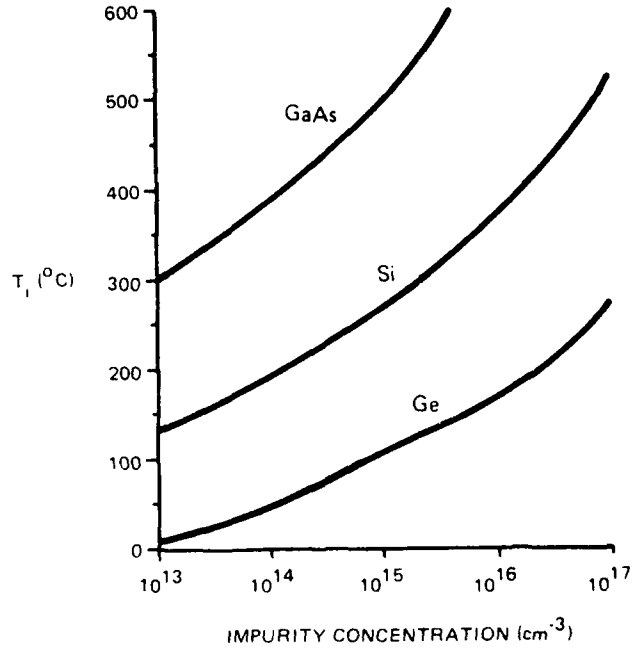


Figure 22. Intrinsic Temperature Versus Doping Level

2. P-N Junctions

a. Low Stress Behavior

1) Reverse Leakage

The reverse leakage of diodes at room temperature is insignificant because leakage current is proportional to the density of minority carriers which is usually very small. As temperature increases, however, the number of minority carriers available for conduction increases significantly. These minority carriers are accelerated across a reverse biased junction, so current is limited only by the number of minority carriers available for conduction. Reverse current consists of a generation component which arises in the depletion region and is given by:

$$I_{gen} = \frac{qA\ n_i W}{\tau}$$

and a diffusion component which is generated at the boundaries of the depletion region and the bulk material and is defined as:

$$I_{diff} = \frac{q\ AL\ n_i^2}{\tau N}$$

where L is the diffusion length of minority carriers.

The diffusion term is often cited as the component that is responsible for instability because of its n_i^2 dependence.

The diffusion leakage current component assumes the absence of an electric field in the regions bounding the depletion region which is not true for a junction in avalanche. In avalanche the electric field induced in the bulk region from the avalanche current will create a drift field in a direction which will direct minority carriers across the junction. When an E-field is present in the bulk regions, it is possible to define a minority carrier resistivity. Plots of the resistivity of silicon due to minority carriers only are given in figures 23 and 24.

2) Breakdown Voltage

If the electric field in the depletion region increases to the point where charges traversing the region are accelerated to energies sufficient to cause impact ionization, the junction will enter into avalance conduction.

As temperature increases, the mean free path between lattice collisions decreases. Since the energy acquired by a carrier is a function of the E-field and its mean free path, fewer carriers acquire sufficient energy for impact ionization at higher temperatures and the ionization coefficient decreases, resulting in an increase in breakdown voltage. The method used to investigate the temperature dependence of breakdown was based on the work of Crowell and Sze (reference 6).

Plots of the ionization coefficients for electrons in silicon for various temperatures are given in figure 25. Breakdown voltage as a function of temperature may be calculated at various doping

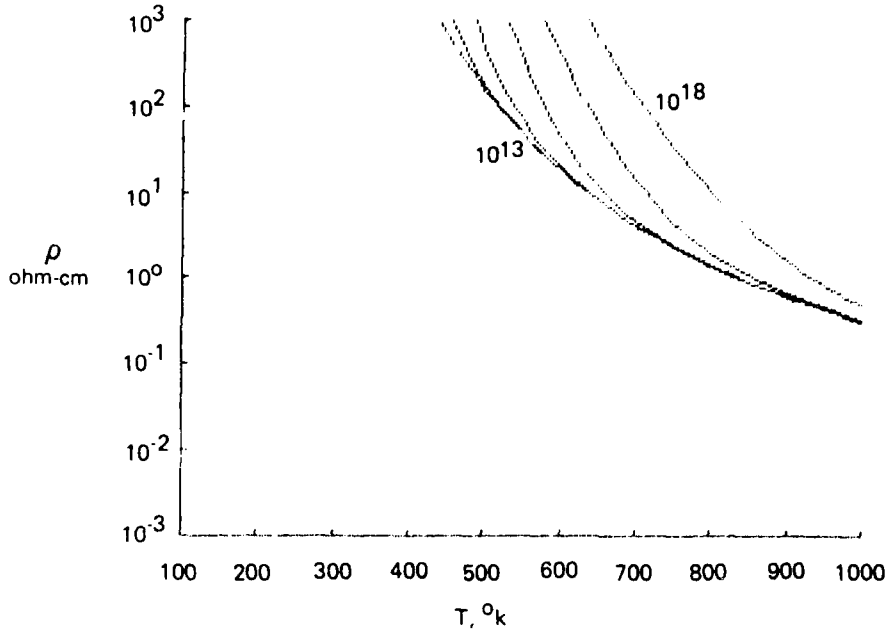


Figure 23. Minority Carrier Component of Resistivity, N-Type

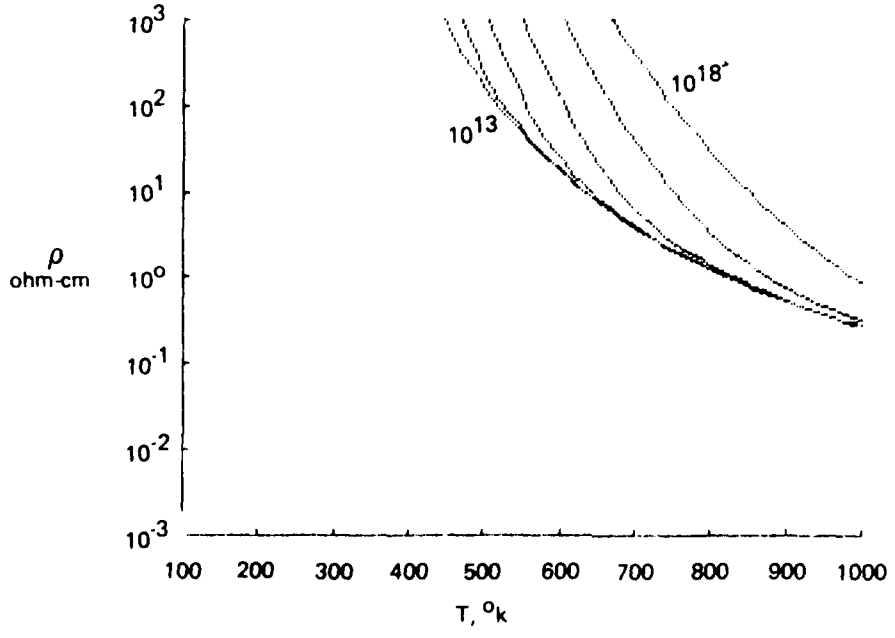


Figure 24. Minority Carrier Component of Resistivity, P-Type

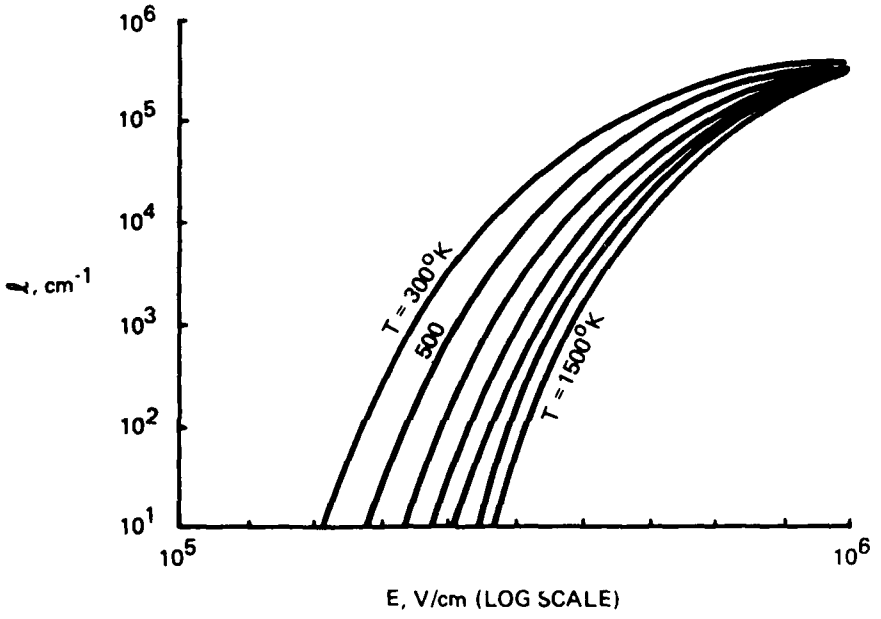


Figure 25. Electron Ionization Coefficient as a Function of E Field

levels by assuming an abrupt one-sided junction (see figure 26). The width of the depletion region of the junction is:

$$W_d = \sqrt{\frac{2\epsilon_s V}{qN}}$$

The electric field for an abrupt junction decreases linearly from a maximum value at the junction to zero at the edge of the depletion region. The maximum value of the electric field is:

$$|E_{max}| = \frac{q N W_d}{\epsilon_s}$$

Breakdown voltages as a function of temperature were investigated by choosing a reverse bias voltage and then integrating an average of the electron and hole ionization coefficients across the depletion region using a 10-step rectangular approximation. If the result of the integration was less than unity, the reverse voltage was incremented and the process was repeated. When the result of the integration exceeded unity, the voltage was taken as the breakdown voltage. Results are shown in figure 27.

Note that the lightly doped diodes are the most temperature sensitive. This phenomenon occurs because the low-field ionization coefficients are also relatively temperature sensitive. Since the lightly doped diodes have relatively wide depletion regions, the low field ionization coefficients are more important than in narrow depletion width diodes.

Breakdown voltage has a positive coefficient with temperature which will tend to stabilize the junction. If one region of the junction is drawing more current than another, that region of the junction will be raised to a higher temperature and the resulting increase in breakdown voltage will tend to divert current away from the region.

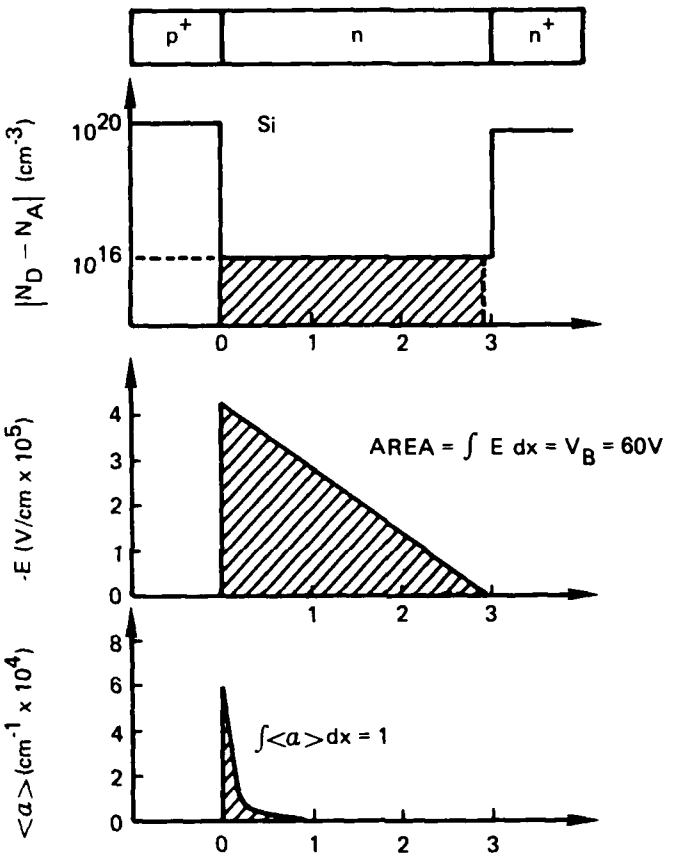


Figure 26. Step Junction Diode Structure

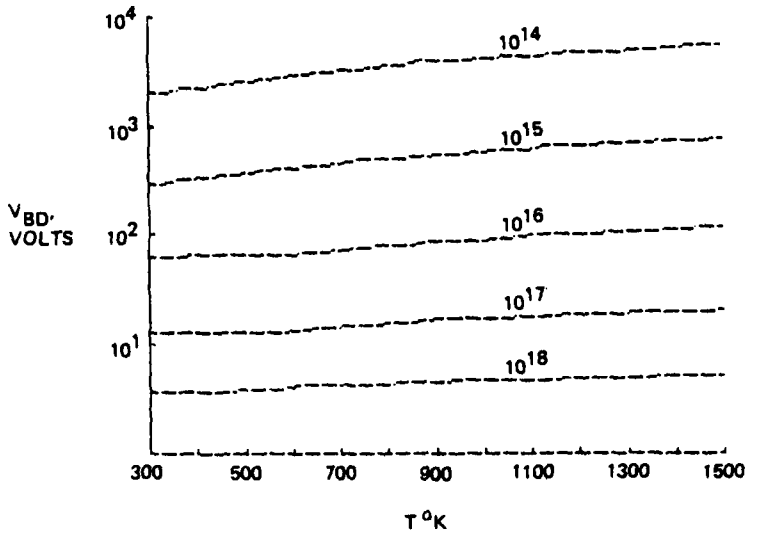


Figure 27. Breakdown Voltage as a Function of Temperature

b. High Stress Behavior

Figure 28 illustrates the electric fields within a P+N-N+ diodes under conditions of increasing reverse bias. The first electric field plot represents the diode under a reverse bias insufficient to cause breakdown. Reverse bias causes holes in the P+ region and electrons in the N- region to be drawn away from the junction region which leaves the bare charges of the fixed, ionized dopant atoms. The electric field within the device is found by integrating this charge across the device. The voltage drop across the device could be found by integrating the electric field and must be precisely equal to the reverse bias voltage. The sum of the positive and negative charges within the device must be equal, so that electrostatic charge neutrality of the device is maintained.

As the reverse bias voltage is increased, the electric field will reach levels sufficient for impact ionization. The avalanche breakdown voltage is reached when the integral of the ionization coefficient across the device (which is highly field dependent) reaches unity. Only the peak field region will contribute significantly to the integral.

When the avalanche breakdown voltage is reached, any attempt to further increase the voltage will greatly increase the device current which will tend to maintain the voltage across the device. To a first approximation, the peak electric field reaches a maximum. An electric field now appears in the bulk region. This electric field represents the voltage drop across the bulk region resulting from the finite resistance of the bulk material.

Since the peak electric field occurs at the junction, electrons will be the principal carrier of charge across the depletion region. Since the electric field in the depletion region exceeds the scattering limited velocity critical field across most of its length, conduction will be space-charge limited. The effect of the excess negative charge will be to increase the electric field in the depletion region as illustrated in figure 28. The disturbance in the electric field may be calculated as:

$$\Delta E = \frac{IX}{A\ \epsilon_s\ V_{SL}}$$

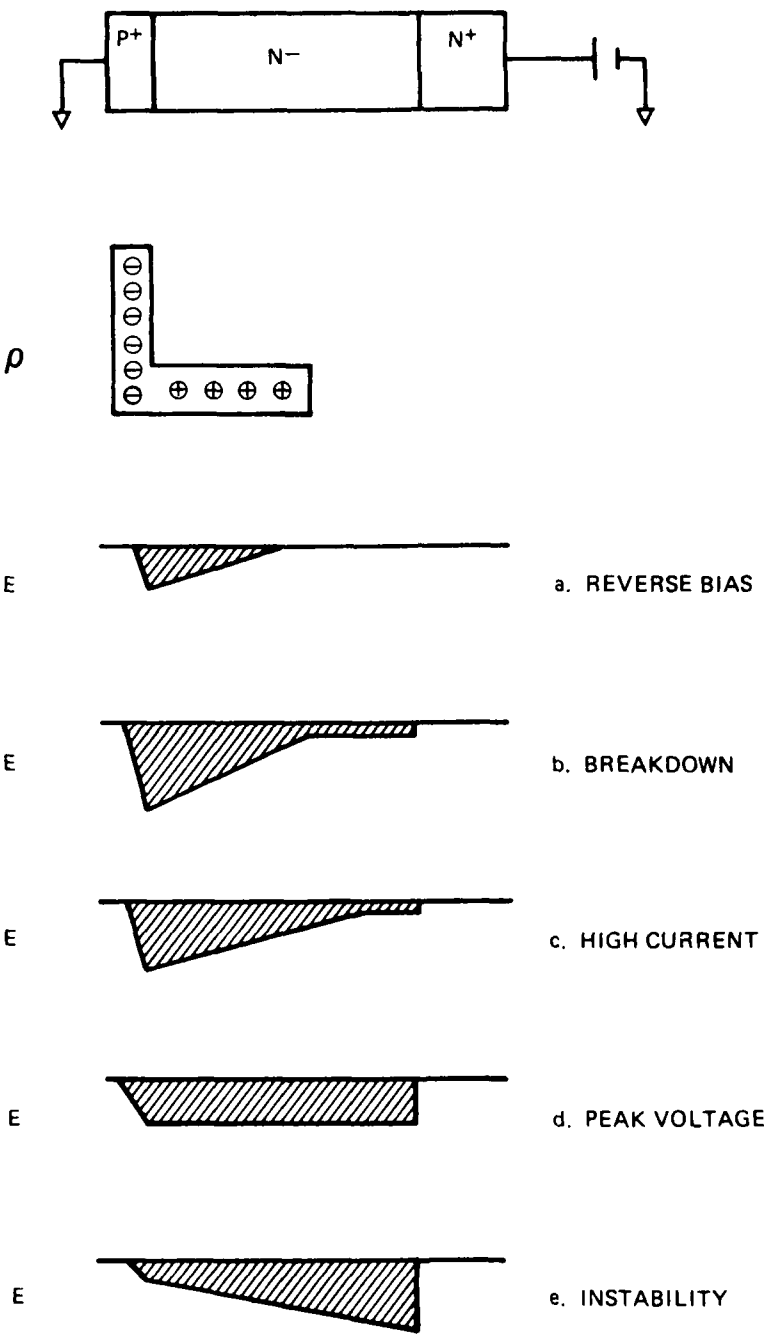


Figure 28. Electronic Instability in a P-N Junction

The increase in the electric field will cause an increase in voltage which could be found by integrating the electric field over the length of the diode. Since the increase in voltage will be proportional to current, the effect may be treated as a parasitic junction resistance and is known as space-charge resistance.

Other effects associated with the space charge are a widening of the depletion region and a decrease in the peak electric field. The reduction in the peak electric field occurs because the fall-off of the electric field is more gradual and hence, the fall-off of the ionization coefficient is less rapid with distance from the junction. Thus, the peak electric field which results in a unity integral of the ionization coefficient over distance will be less.

At higher current densities, the depletion region will spread to the N+ region where it will effectively stop. Further increases in current will still continue to cause the electric field to "even out". Eventually, the electric field will become uniform from the junction to the N+ region. When this occurs, avalanche injection of holes at the N+ region will become significant. The holes will reduce the electric field in the interior portions of the depletion region allowing more current to flow. The device has now entered a region of negative resistance. Note that the situation in figure 28 is similar to bulk material at the onset of instability. The situation is also similar to a P-I-N configuration whose negative resistance characteristic is often utilized as an oscillator.

3. Failure Models

The modeling of the electro-thermal behavior of integrated circuit structures requires a criterion to determine when a simulated failure has occurred. Failure was assumed under the following conditions:

(1) The device reached the melting point of its material.

(2) The surface temperature exceeded the eutectic point associated with silicon and the surface metal with which it is in contact.

D. LIMITING FACTORS OF ALUMINUM INTERCONNECTS

Two aluminum interconnect models were chosen for investigation, an adiabatic model described only by a cross-sectional area and a two-dimensional model simulating an interconnect with a right angle turn. The purpose of the two-dimensional model was to investigate the effect of nonuniform E-fields on the heating process.

The adiabatic aluminum interconnect model is shown in figure 29. The resistance of the interconnect is assumed to be small compared to the 150-ohm source resistance of the ESD threat, so the electrical portion of the model consists of only the ESD capacitance and source resistance. The thermal portion of the model consists of a current source and a capacitor. The current source was set equal to the power which would be dissipated in a unit length of interconnect at a fixed area when driven by an electrical current equal to the electrical current flow through the ESD resistance.

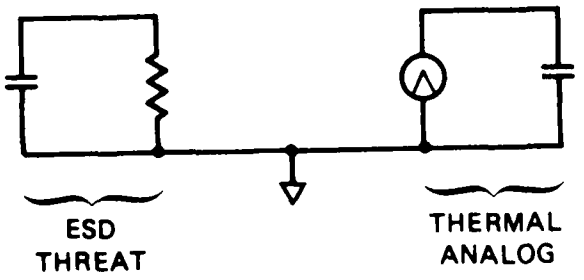


Figure 29. One-Dimensional Aluminum Interconnect Model

The thermal model capacitor was set equal to the specific heat of a unit length of interconnect. The voltage across the thermal model capacitor was proportional to the temperature of the interconnect. The initial value of the capacitor voltage was set to 300 volts to simulate an ESD event occurring at room temperature. Since the resistivity of the aluminum interconnect varies with temperature, provisions were made to

continually vary the output of the current source based on the temperature of the interconnect and the current flowing through the ESD threat electrical circuit. The buildup of heat in the interconnect model was assumed to be an adiabatic process where no heat energy leaves the interconnect. The thermal diffusion length of silicon dioxide after one Human Body ESD time constant of 22.5 nS is only about 0.1 microns which supports the adiabatic assumption. Lateral heat flow was found to be negligible.

Simulated failure was obtained at an interconnect cross-sectional area of 1.6×10^{-7} cm^2 when driven by the "Human Body" ESD model. The "Device Charge/Discharge" ESD model produced a simulated failure when the area reached 1×10^{-7} cm^2. Thus, a minimum cross-sectional area of 1.7×10^{-7} cm^2 is required to withstand typical ESD events. For an aluminum film thickness of 1 micron, this implies that a minimum width of 17 microns for ESD survivability is required on lines directly connected to input or output pins.

The two-dimensional aluminum interconnect model is shown in figures 30 and 31. This model was created to study the effect of variations in geometry, in this case a right angle turn. Simulations were made at an interconnect thickness of 1 micron and an initial width which did not yield a simulated device failure. The initial temperature of the thermal analog was set to room temperature ($300^{o}K$). The width was then reduced incrementally until a portion of the model reached the melting temperature of aluminum.

Simulated failure of the interconnect model occurred when the width was reduced to 20 microns. A plot showing isothermal contours at the failure point is given in figure 32. As expected, the failure point was the inside corner of the turn.

Interpretation of the simulation results is somewhat difficult. Since a molten interconnect corner may not destroy the integrated circuit, and since the outside corner of the interconnect is the coolest region of the interconnect, there is some question as to whether a right angle interconnect turn is harder or softer than a straight section.

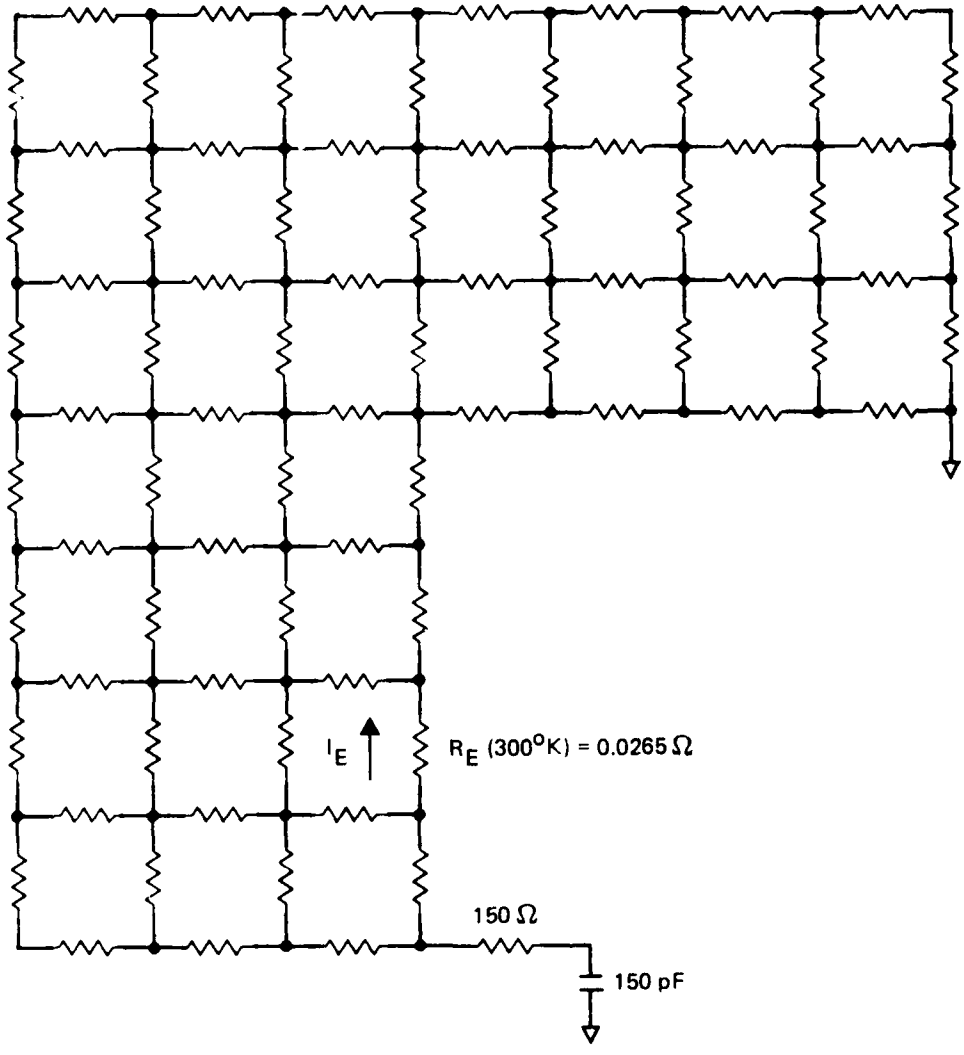


Figure 30. Electrical Response Portion of Two-Dimensional Aluminum Interconnect

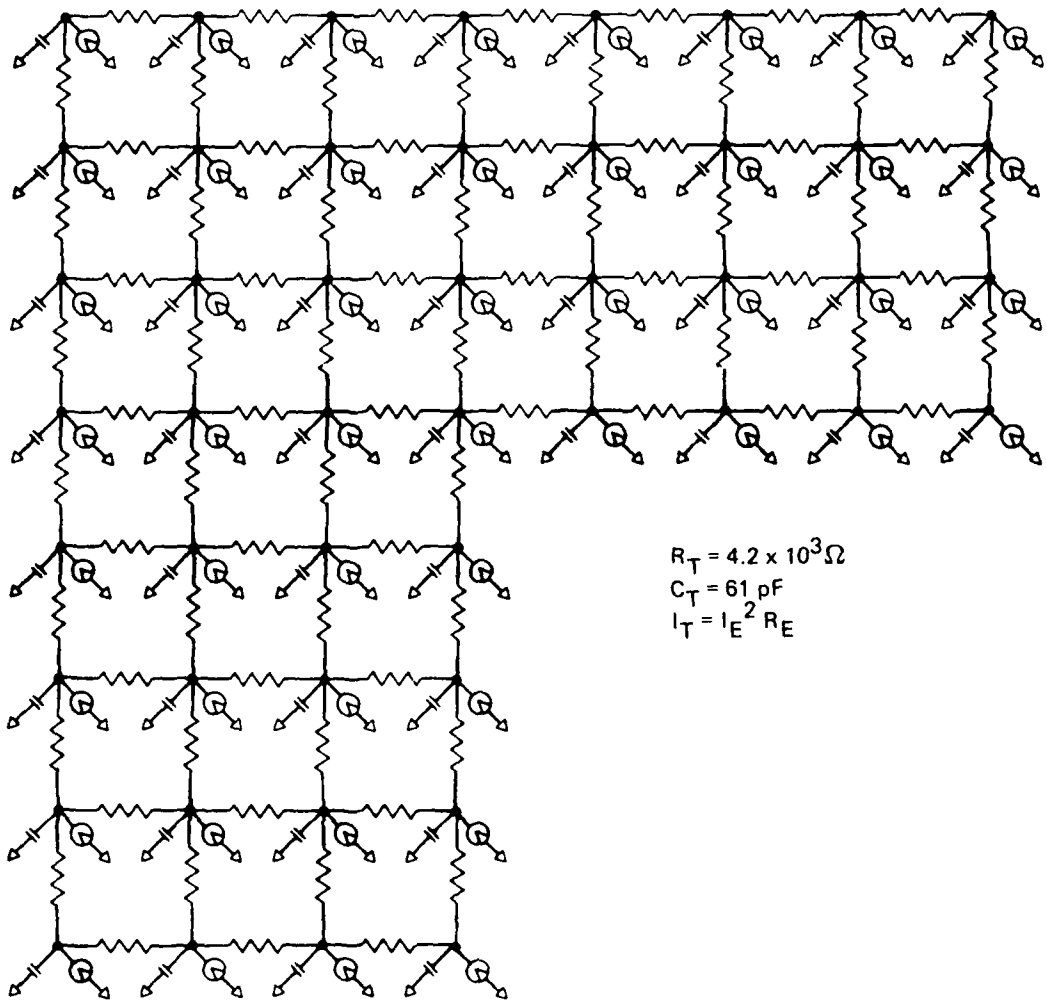


Figure 31. Thermal Analog Portion of Two-Dimensional Aluminum Interconnect

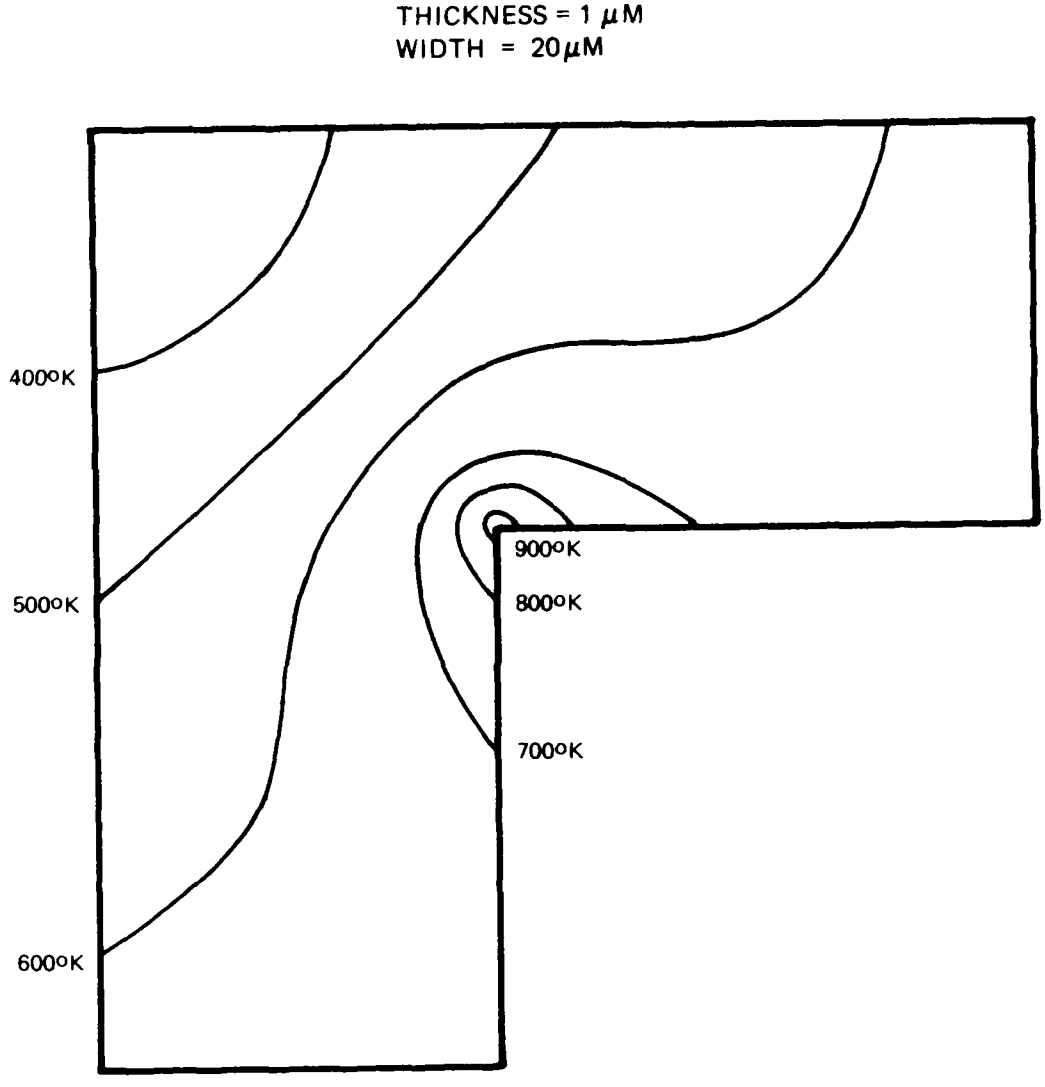


Figure 32. Contours of Constant Temperature During Human Body ESD Event

E. LIMITING FACTORS OF POLYSILICON INTERCONNECTS

For the case where the interconnect resistance is much less than the source resistance, the limiting factors of the interconnect were investigated using the same approach as for aluminum interconnects. The limiting area which could withstand a Human Body ESD and Device Charge-Discharge ESD were found for 0.001 and 0.01 ohm-cm polysilicon. The results of the simulation runs, presented in table 3, may be summarized by stating that the minimum cross-sectional area of a low resistance polysilicon interconnect is capable of withstanding a typical ESD event is about 8×10^{-6} square centimeters.

TABLE 3. LIMITING FACTORS FOR POLYSILICON INTERCONNECT

MINIMUM CROSS-SECTIONAL AREA REQUIRED (cm^2)

RESISTIVITY	THREAT: HB	THREAT: C/D
0.1	8.0×10^{-6}	5.0×10^{-6}
0.001	2.4×10^{-6}	1.5×10^{-6}

F. LIMITING FACTORS OF SILICON DEVICES

There are two distinct methods of initiating failure in bulk and junction semiconductor devices, by heating the device to the intrinsic temperature associated with its doping characteristic or by inducing unstable double injection by forcing excessive current through the device. Either method will result in current constricting into a narrow intensely heated channel where destructive melting may occur.

Thermal instability results when the semiconductor is heated to the point where the intrinsic carrier concentration approaches the doping

concentration of the lightly doped regions of the semiconductor. When the intrinsic temperature is reached, generation and diffusion currents have a positive coefficient with temperature and thermal runaway of the generation and diffusion currents may occur.

Current mode instability occurs when the device current density exceeds the background doping concentration of the lightly doped regions of the device. When this condition occurs, conduction is space-charge limited, and the E-field within the semiconductor increases. If the E-field reaches the critical field for impact ionization, double injection will result, and current flow will become unstable, forming a narrow constriction where destructive heating may occur. The maximum E-field in the device depends on the doping concentration, the current density, and the length of material in space-charge limited conduction. If the region is short, the device may operate well into space-charge limited conduction without the E-field reaching values that would result in double injection and instability. If the region is infinitely long, double injection conditions will occur at the same current density where space-charge limited condition occurs. Conservatively, any device is threatened with current mode instability when the current density through the device exceeds the threshold for space-charge limited conduction.

One method for limiting the length of a region in space-charge limited conduction is to terminate the region in a higher doping. For example, an N+N-N+ device where the N- region is narrow could tolerate much higher currents than the same device where the N- region is wide.

Another method for limiting the length of a region is through the use of a punch-through structure. A punch-through structure is an N+P-N+ or P+N-P+ device where the lightly doped regions are very narrow. If the depletion region spreads across the lightly doped region before breakdown fields are reached, the two heavily doped regions are effectively connected together and a large current will flow. Conduction in the lightly doped region will be space-charge limited.

Because the ESD event is associated with very high current densities and very short pulsewidths, electronic instability is the most likely

candidate for initiating device failure. Since electronic instability cannot occur below current densities where bulk semiconductor conduction is not space-charge limited, the safe operating region may be described as a plot of the critical current density for space-charge limited conduction versus background doping as illustrated in figure 33. The peak current for the standard "Human Body" ESD model is about 27 amperes and a plot of the minimum area which is capable of withstanding the "Human Body" ESD event is given as figure 34.

Electronic and thermal instability were investigated for longer pulsewidths through the use of circuits analogs of heat flow in a hypothetical device. The circuit analog applied is shown in figure 35 and represents a bar of silicon of one square centimeter and a finite length. The current source represents the deposition of power at the surface of the bar. The capacitors model the specific heat of silicon, and the resistors model the temperature dependent thermal resistivity. Each R-C lump represents a portion of the length of the bar. The lengths chosen increase exponentially since the transient temperature profile is roughly exponential in form. Depending upon the pulsewidth investigated, the total bar length was selected so that the last lump temperatures would rise only a few degrees during the simulation. For pulsewidths of 1ØØ nS, a length of 1Ø um was chosen, for pulsewidths of 1 uS, a length of 3.16 uM was chosen, and for a pulsewidth of 1Ø uS, a length of 1ØØ uM was chosen. Note that length was increased proportionally by the square root of the pulsedwith.

The model was exercised at the three pulsewidths using various values of the current analog of power. Plots of the simulation results giving the peak temperature (voltage of the first lump) are shown in figure 36. Note that the power required to produce a constant peak final temperature varies inversely with the square root of the pulsewidth. This is a simulation verification of the Wunsch expression which describes the power required to fail a device as being proportional to time raised to the minus one-half power.

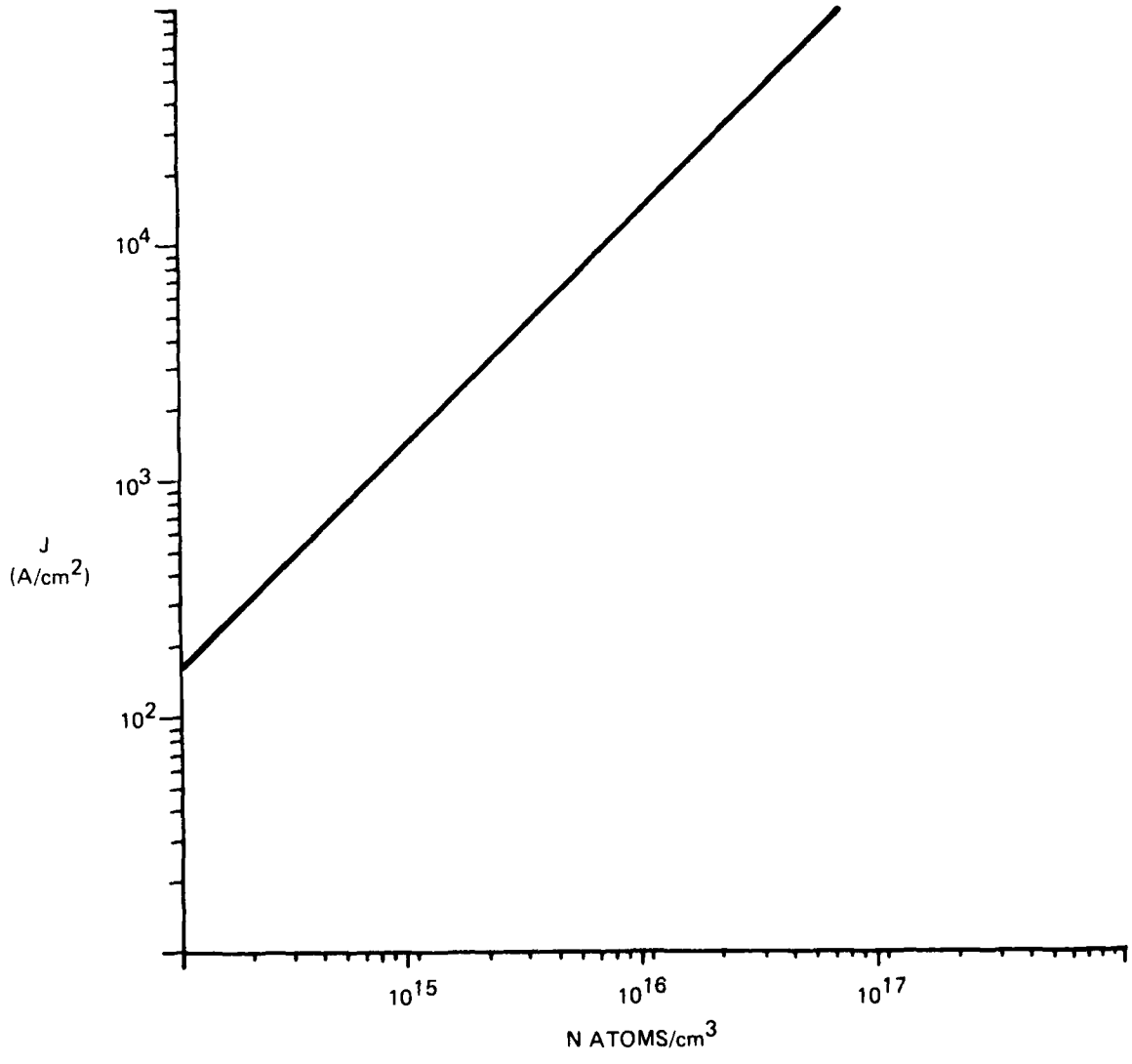


Figure 33. Critical Current Density for the Onset of Electronic Instability as a Function of Doping Level

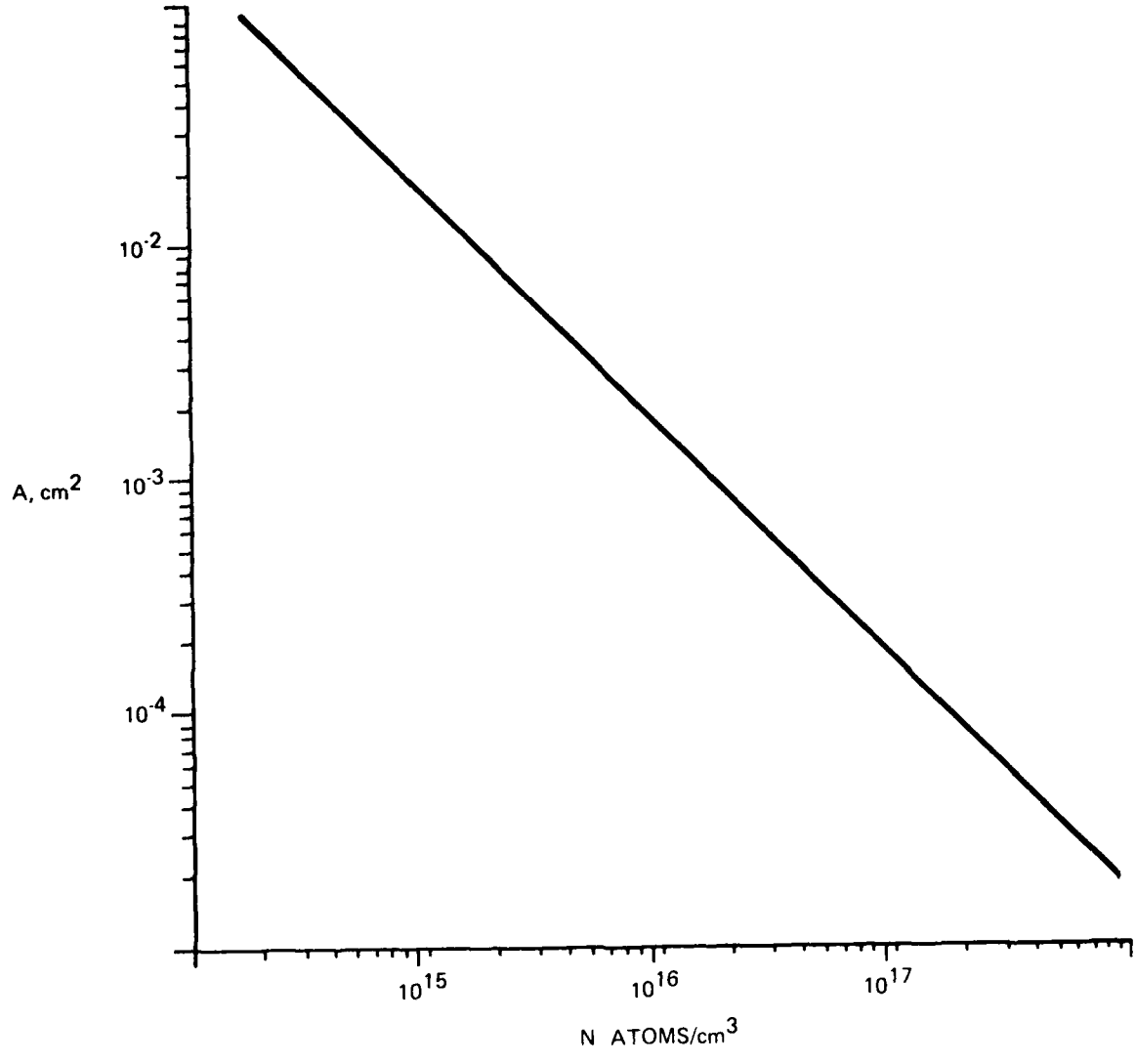


Figure 34. Limiting Device Area for Prevention of Instability for Standard "Human Body" ESD Event as a Function of Doping Concentration

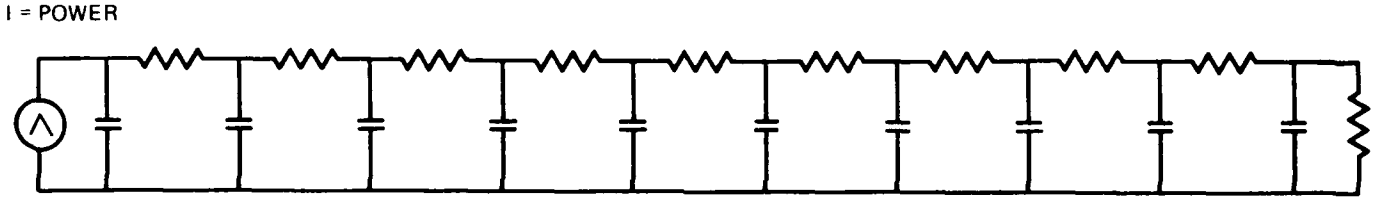


Figure 35. Thermal Analog of p-n Junction

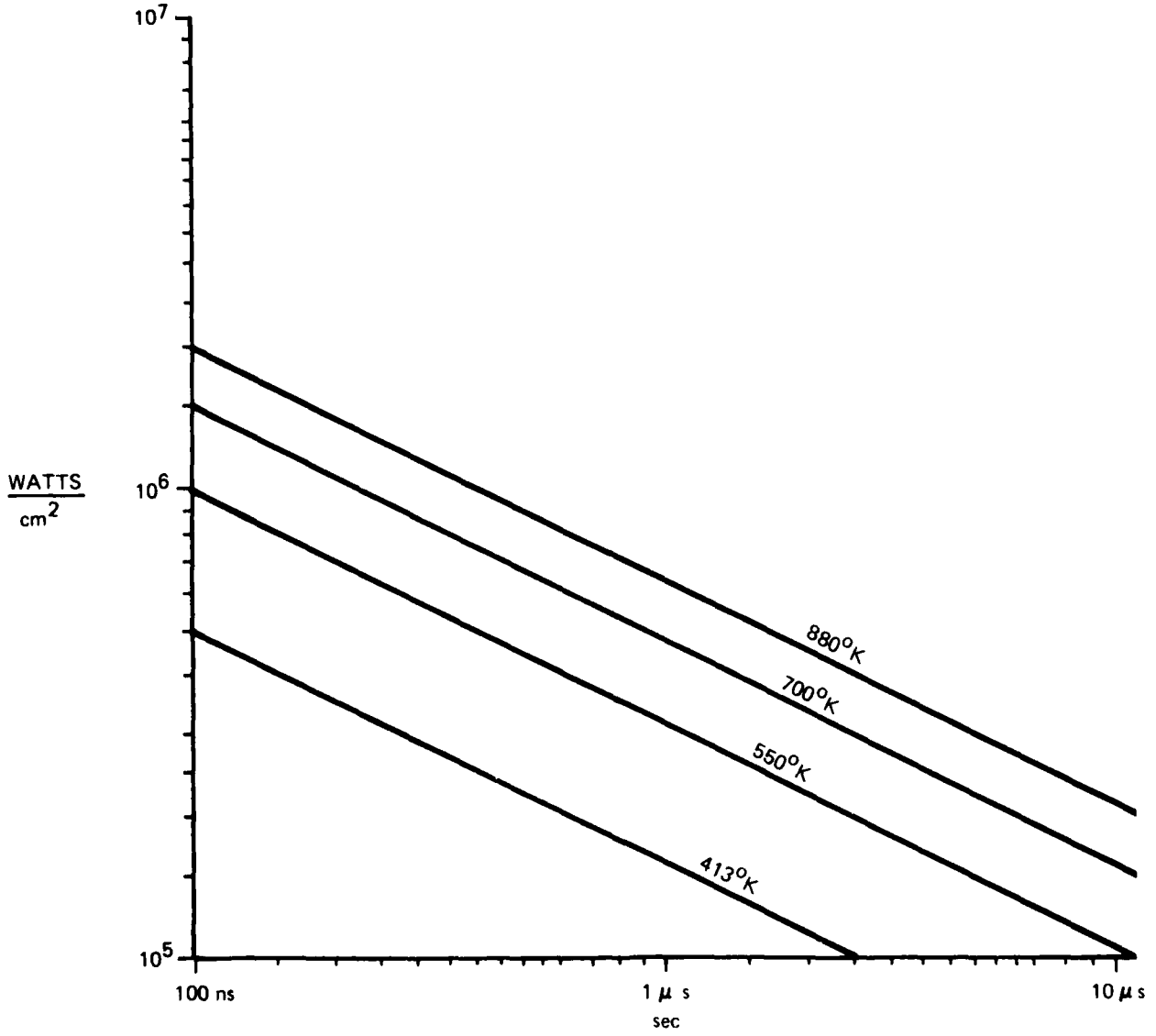


Figure 36. Peak Temperature as a Function of Power Density and Pulse Width for a Shallow Junction

Three of the four isothermal curves shown in figure 36 are fortuitously close to the intrinsic temperature of silicon doped at ten to the 15, 16, and 17 power. Since each background doping concentration has a corresponding breakdown voltage and since power dissipation in a junction device can be estimated as the product of breakdown voltage times current, the current density to produce the required power density to heat a given doping level to the intrinsic temperature can be found.

Figure 37 is a composite plot of the critical current density required to initiate electronic or thermal instability as a function of pulsewidth for three doping levels. The horizontal lines in figure 37 represent the current density at which bulk space charge conduction occurs and represents the approximate onset of purely electronic instability. The diagonal line intersecting the space charge conduction current limit near the center of the plots represents the family of points where the device will be heated to the intrinsic temperature. The curve line which smooths the intersection between the electronic and thermal failure lines represents the family of points where the device will be heated until the space charge limited velocity falls to the point where electronic instability will be initiated.

The plots contain several interesting features. For example, the highly doped devices can withstand a much higher current density than the lightly doped devices. Also, current mode instability should initiate failure for all three doping levels investigated at pulsewidths below 100 nS, while thermal instability should initiate failure for pulsewidths greater than 1 uS. Since ESD pulses are usually shorter than 100 nS, current mode instability is expected to be the dominant failure mode.

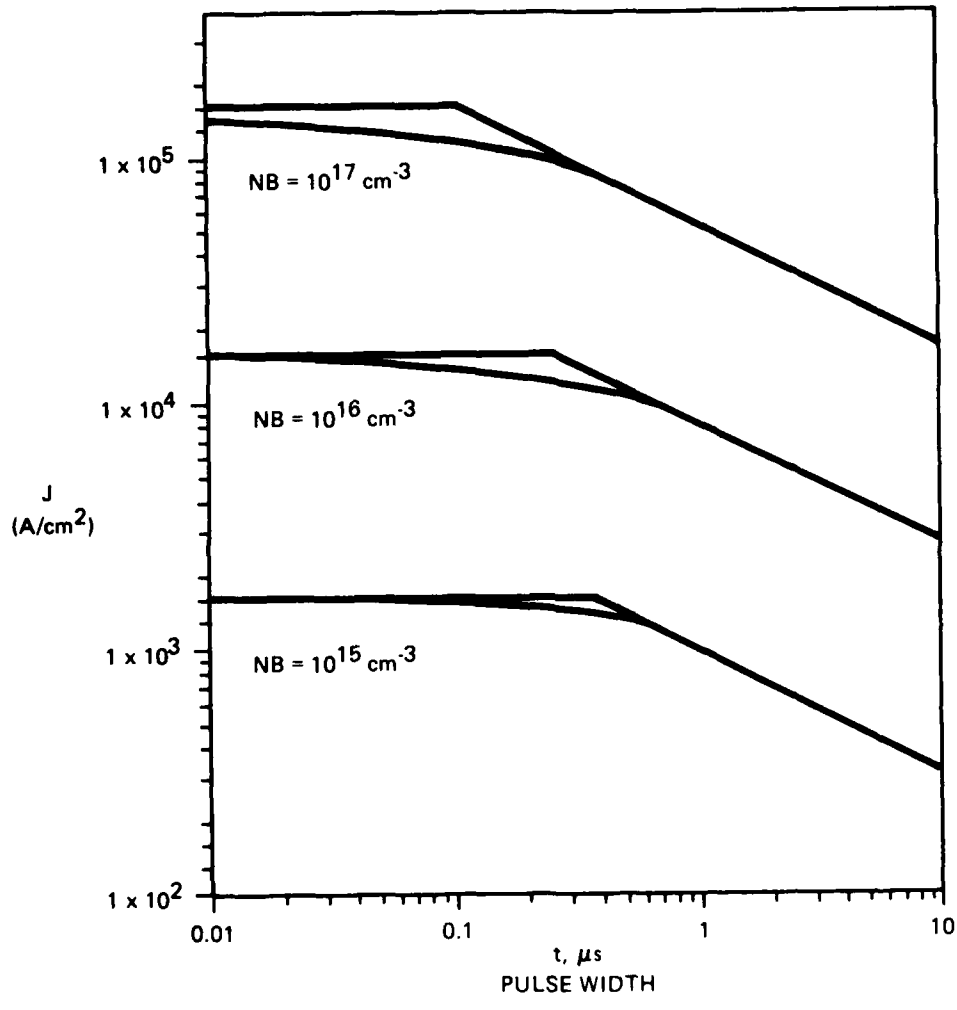


Figure 37. Current Density Required to Induce Second Breakdown

SECTION VII
RESULTS OF VERIFICATION TESTS

A. NPN TRANSISTOR

The NPN transistor investigated was fabricated as part of the Component Statistical Characterization Program. The fabrication masks for the transistor are illustrated in figure 38 and process data are given in table 4. The electrical overstress characterization consisted of three step-stress test series. The test configurations are depicted in figure 39. The power required to produce failure was found to fit the expression: $P=21.9t^{-0.44}$ where t is in microseconds.

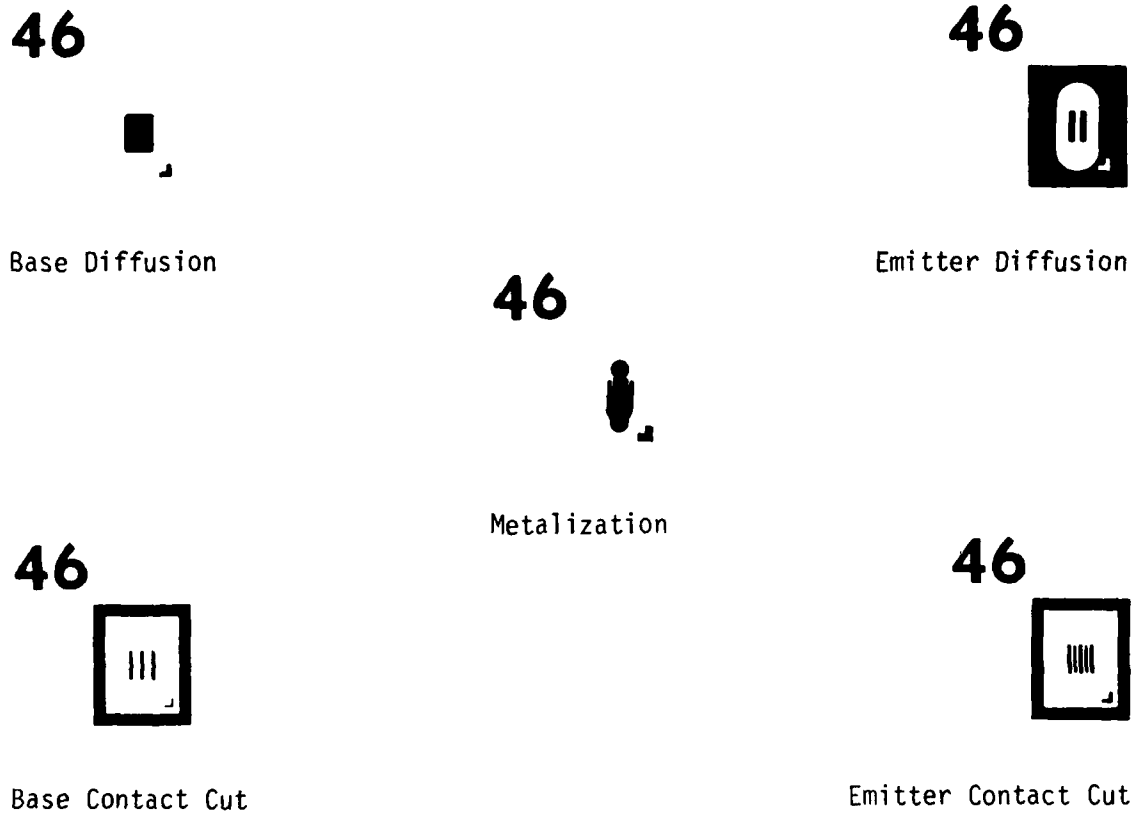


Figure 38. Process Masks

TABLE 4. TRANSISTOR DATA

Emitter Base			Collector Base		
Area	Perimeter		Area	Junction Perimeter	Contact Perimeter
3.89×10^{-5}	4.8×10^{-2}		1.21×10^{-4}	4.35×10^{-2}	6.6×10^{-1}
BETA	BVEBO (V)	BVCBO (V)	COEB (Pf)	COCB (Pf)	TRANSIT TIME (ns)
60.6	6.42	107	4.13	2.81	0.774

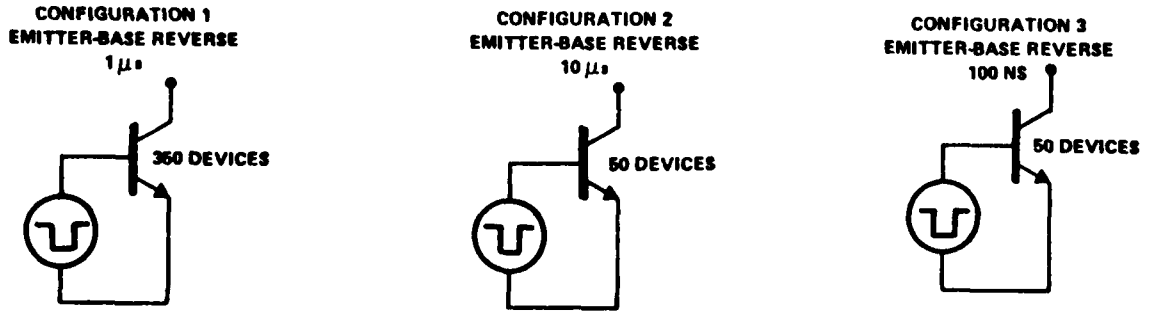


Figure 39. Test Configurations

The power required to produce failure at 10, 1 and 0.1 microseconds was found by substituting time in the previous expression. The power density required to produce failure at a given pulsewidth was then found by dividing the failure power by the emitter-base junction area. The assumption is that current is uniform within the emitter. From the curves of figure 36, the peak junction temperature is expected to be about 880 K. This corresponds to the intrinsic doping range of about $2x10^{17}$. The doping concentration in the base, as estimated from breakdown voltage, is $3x10^{17}$, which is in good agreement. Thus, the failure characteristics of an actual transistor and the theoretical failure characteristics derived while investigating limiting factors were found to be consistent.

B. 1N4003

To investigate the behavior of devices under stress more closely resembling ESD, several 1N4003 rectifier diodes were tested in the BDM R&D lab with an SPG-200 pulser. The SPG-200 delivers its pulses by the relay activated discharge of a length of 50-ohm coaxial cable which has been charged to a given value by a high voltage power supply. For this test, the short internal length of cable proved to be long enough. From time domain reflectometry tests, the charged cable was found to have an effective length of 45 centimeters which will deliver a pulse 3nS long into a 50-ohm laod.

The 1N4003 was assumed to be a one-sided abrupt junction. The doping concentration of the lightly doped side of the junction was estimated from the breakdown voltage of the diode as $3x10^{14}$. The area of the junction was estimated from the doping concentration and the junction capacitance data given in the manufacturer's specification sheets. Curves which plot capacitance per unit area versus doping concentration for various reverse bias voltages indicate that the active area of the diode was 0.014 cm^2. The width of the depletion region at breakdown bias

voltage is a function of doping concentration and was estimated at $3x10^{-3}$ cm.

The charged coaxial line of the pulse has approximately 1 picofarad of capacitance per centimeter. The maximum voltage utilized in the test procedure was 6 kV. Therefore, the maximum energy which could be delivered is 0.81 mJ.

If the total energy of 0.81 mJ is deposited in the depletion volume of $4.2x10^{-5}$ cm^3, the temperature will rise only 12 degrees which is not sufficient to cause failure. The intrinsic temperature of silicon doped to $3x10^{14}$ is about 500 K or a temperature rise of 200 degrees. The junction area of a 1N4003 which would produce a 200 degree rise after absorbing 0.81 mJ of energy is $8.2x10^{-4}$ cm^2 which is 17 times smaller than the estimated area. Yet, failures were obtained with energies less than 0.81 mJ if the devices were reverse biased above a threshold reverse bias. This suggests that the pulse may have produced a nondestructive current instability, and if the bias was sufficiently high, the bias current destroyed the device.

From figure 33, the critical current density required to initiate electronic instability for a doping of $3x10^{14}$ and area of 0.014 cm is about ($478A/cm^2$) (0.014 cm^2) or 6.7 amperes. A rough estimate of the peak current supplied to the device from the SPG-200 charge line pulser is 100 amperes. Therefore, the SPG pulser could easily supply the current required to initiate a current mode instability which would short the junction. Once initiated, the instability would cause the voltage across the device to collapse. The remaining energy in the pulser may or may not be sufficient to cause melting in the resulting current constriction. From the experimental data, it would appear that the SPG-200 does not have enough energy to destroy the device after inducing instability. However, if sufficient bias is applied, the current which flows through the device, after the instability is induced, will sustain the instability and deliver enough power to the current constriction to destroy the device. This experiment seems to verify the current-induced instability calculations found in the limiting factors study.

C. SOS DIODE

A test vehicle chosen to aid in the investigation of the limiting factors are expected to determine the electrical overstress sensitivity of micron and submicron technologies was a silicon-on-sapphire diode which was fabricated in support of the DNA Electrical Overstress Program (reference 10). The SOS diode was used to study the fundamental physical mechanisms of electrical overstress.

The SOS diode was a P-N-N+ diode fabricated using silicon-on-sapphire technology. The topology and process parameters on the diode are given in figure 40. The diode construction allows light to pass through the structure. The transmittivity of light through the structure is a function of the density of free electrons which in turn is a function of lattice temperature. By pulsing the diode and stroboscopically examining the diode at a given time during the pulse, the thermal behavior as a function of time can be deduced.

$N_D^- = 1 \times 10^{17}/cm^3$
THICKNESS = 0.4 μM

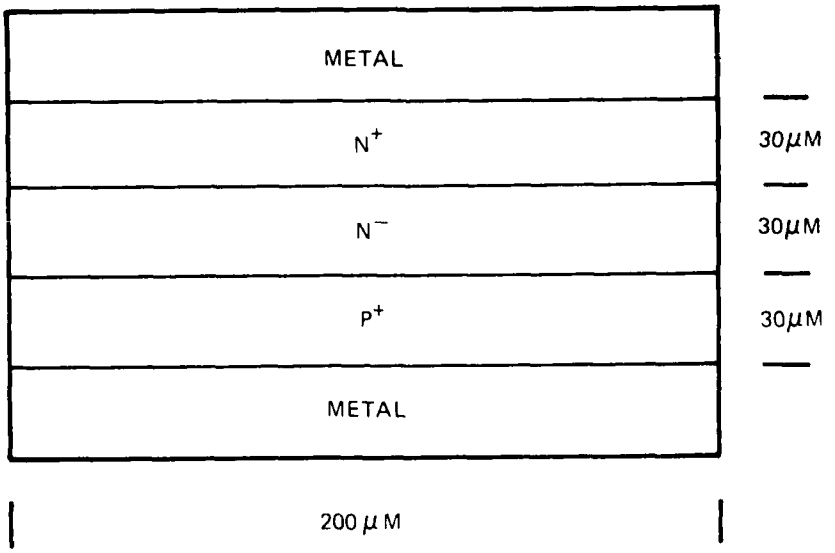


Figure 40. SOS Diode Topology

The test shows that instabilities, in the form of hot spots, developed along the junction. Figure 41 shows the current and voltage waveforms for a test along with photographs of the device before and at the end of the pulse.

The device current which separates the low field region from the high field region is:

$$I = AqV_{SL}N$$

For the SOS diode, the boundary current is 0.13 amperes which is greater than the drive current. Therefore, the SOS diode was modeled using low field device theory.

The SOS diode was assumed to fail by being heated to the intrinsic temperature of about 500°C. The breakdown voltage of the SOS diode was about 12 volts and the bulk resistance was about 375 ohms. At a constant current at 0.1 ampere, about 1.2 watts were dissipated in the junction and about 3.75 watts were dissipated in the bulk region. Photographs in the early stage of heating show the temperature to be fairly uniform across the device; therefore, the hypothesis was that bulk heating was the primary failure mechanism.

An equivalent circuit model was developed to simulate the electrical and thermal properties of the bulk N-type material. The equivalent circuit model is shown in figure 42. The electrical portion of the model consists of a current source in series with a resistor. The current source was set at 0.1 ampere and modeled the current drive. The resistor modeled the resistance of the bulk region of the diode as a function of temperature. The thermal portion of the model consisted of a current source in parallel with a resistor and a capacitor. The current source was set equal to the electrical power dissipated in the bulk resistance. The resistor and capacitor modeled the thermal resistance and capacitance of the sapphire substrate respectively. The contribution of the thin silicon film to the thermal model was assumed to be negligible.

Before Stress

During Stress

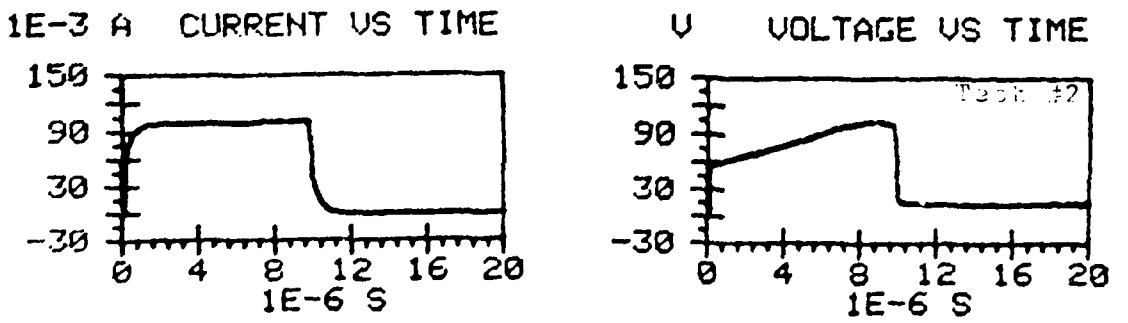


Figure 41. SOS Diode Stress Test

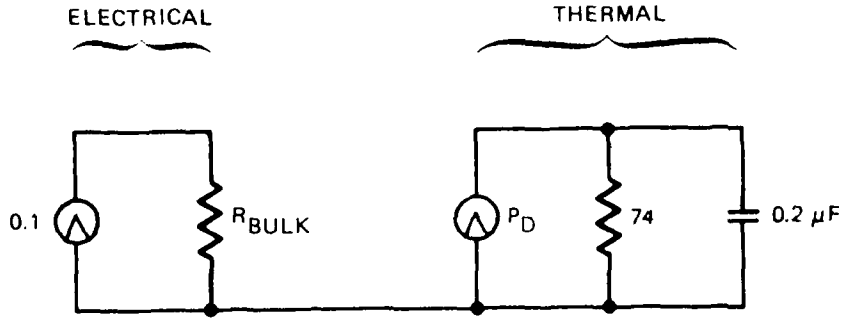


Figure 42. SOS Diode Model

The thermal resistance and the thermal capacity of the sapphire substrate were estimated by first calculating the depth to which heat will flow into the substrate. The thermal resistance and thermal capacitance product determine a time constant which if set to the pulsewidth of 10 uS can yield the thermal diffusion length.

$$RC = 10us = (PL/A)\ (SV)$$

where P is the thermal resistivity of the sapphire, L is the depth of heating, A is device area, S is the specific heat of sapphire, and V is the heated volume of sapphire. Substituting:

$$10uS = (PL/A)\ (SAL) \approx PSL^2 = 14.7\ L^2$$

$$L = 8.25 \text{ microns} \qquad 10 \text{ microns}$$

The thermal resistance of a slab of sapphire with an area of 0.6 square microns and a depth of 10 microns is about 74 ohms while the thermal capacity of the same slab of sapphire is about 0.2 microfarad.

The voltage across the bulk resistance was monitored during the simulation. As temperature increased, the intrinsic temperature was eventually reached and the bulk resistance began to decrease with time. In a real device, a negative coefficient of bulk resistance with temperature would result in unstable current.

A plot of simulated voltage across the bulk region of the diode plus the breakdown voltage together with the experimental result is shown in figure 43. The simulation predicts instability in 10us which is in good agreement with the observed results. However, the peak observed voltage is much lower than the peak simulated voltage. The discrepancy is possibly attributable to the effects of nonuniform current flow and heat buildup at the junction which will cause instabilities in a real device to develop much earlier than predicted by simulation.

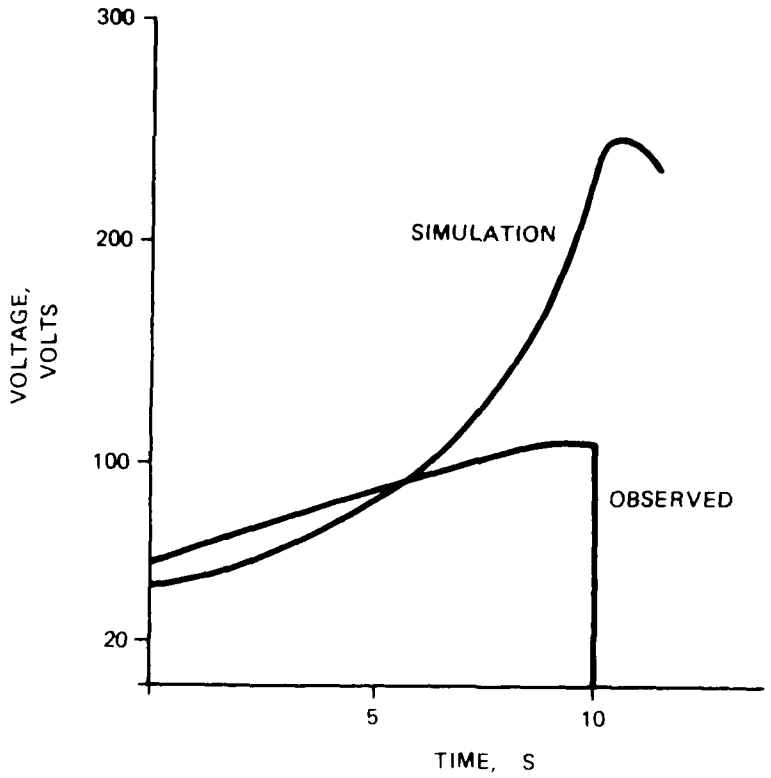


Figure 43. Investigation Results

SECTION VIII

PROTECTION NETWORK FOR NMOS TECHNOLOGY ICS

Two building blocks available for the design of input protection networks are series and shunt impedance elements. A series impedance element will limit the ESD surge current, thereby easing the design requirements of subsequent shunt impedance elements. Protection against ESD will increase with series impedance. However, circuit performance will decrease since a series resistance will increase the time required for a logic signal to charge gate and parasitic capacitance.

An upper limit to the series resistance can be established from the dielectric strength of the field oxide. If the NMOS process of table 1 is chosen as a design baseline, the maximum voltage appearing on a series resistor must not destroy a 3500-angstrom field oxide. Assuming a dielectric strength of 6 MV/cm, the maximum voltage will be 210 volts. The maximum series resistance can be calculated as the resistance following 4 kV and 150 ohms which will yield a divided voltage of 210 volts. The maximum series resistance is 8.31 ohms. Since 8 ohms is much less than the baseline 150-ohm source resistance, and since the trend in NMOS is toward thinner field oxides, it appears that the series resistance can be dispensed with entirely with few ill effects. Dispensing with the series resistance also eases the problem of parasitic loading of the input signal.

Another advantage of designing a protection network with low impedance shunt elements is the possibility of allowing the protection network to absorb lower amounts of energy. If the impedance of the input protection network is large compared to the 150-ohm source impedance of the baseline ESD model, the bulk of the 1.2 mJ ESD energy will be dissipated in the protection network. If the impedance of the protection network is small compared to the 150-ohm source impedance, the bulk of the energy will be harmlessly dissipated in the source impedance.

Since our baseline transistor has a maximum gate voltage of 21 volts and our baseline ESD model has a peak surge current of 26 amperes, the

shunt resistance has a maximum value of 0.8 ohms or approximately 1 ohm, a very severe design requirement. Two possibilities for low impedance shunt elements are reach-through or punch-through using an expitaxial layer with a heavily doped substrate. Conduction in a punch-through or an avalanching reach-through device will be space-charge limited. Assuming a practical minimum expitaxial thickness of only 1 micron, the device area required to achieve 1 ohm of space-charge resistance is about 4.7×10^{-4} square centimeters or 217 microns on a side. Since space charge resistance increases with the square of the device thickness, thicker epitaxial layers will require much larger areas.

Since a typical bonding pad is 100 microns on a side, even a highly optimized punch-through or reach-through diode will require considerable amounts of integrated circuit area. This drawback together with the requirement for special epitaxial wafers limits the desirability of this approach.

An alternate approach is a device consisting of two source/drain diffusions separated by a distance on the order of a micron as shown in figure 44. One diffusion is connected to the protected node while the other diffusion is grounded. An enhancement mode transistor ion implant has increased the substrate doping near the surface so the depletion region is distorted near the surface. Breakdown will occur at the surface and punch-through will occur below the surface in the substrate. Assuming a surface doping of 2.7×10^{17}, breakdown will occur at about 7 volts.

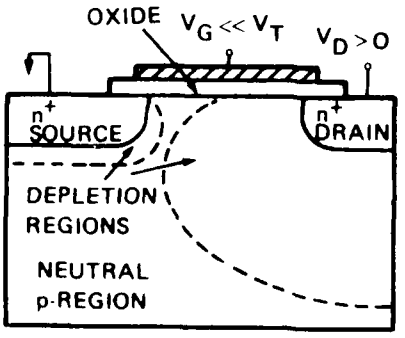


Figure 44. Closely Spaced Diffusions

If punch-through occurs first, a space-charge limited current will flow between the drain and source diffusions. If the voltage is increased to 7 volts, surface breakdown will occur reducing the space charge and initiating avalanche injection. If breakdown occurs first, parasitic NPN transistor action will initiate breakover.

Once breakover has been initiated, the lightly doped P region between the avalanche region and the "emitter" will be flooded with electrons and holes and will behave like a low resistance semiconductor which is indistinguishable from avalanche injection. Thus, the device voltage will not be gain controlled (BVceo), a result which has been verified by Sandia Laboratories (reference 9).

Sandia observed that the sustaining voltage in the low impedance mode of operation was virtually independent of source/drain doping, substrate doping, minority carrier lifetime or channel width with a typical sustaining voltage of 10 volts. Since the breakdown voltage of the device is less than or approximately equal to the sustaining voltage for avalanche injection, the microplasma should be sustained along the entire length of an input protection device.

A thermal analog of the structure shown in figure 45 was developed to estimate the length of the device required to avoid heating to the melting point of silicon. Each lump of the thermal model represents a 1-micron-thick concentric region around the heated volume. The heated volume was assumed to have a radius of 1 micron and a voltage drop of 10 volts. The current source which drove the thermal portion of the model had a value equal to the current flowing through the 150 ohm resistor times ten volts. Resistor values were calculated based on silicon slabs of one micron thickness and area equal to the smaller area of each concentric surface. Each succeeding resistor has a smaller value of each concentric region. Succeeding capacitors increased in value. When driven with the baseline Human Body ESD model, the length required to avoid a silicon melt was found to lie between 500 and 600 microns and the length required to avoid the silicon-aluminum eutectic temperature of 577^{o}C was 1,000 microns.

A conceptual drawing of the topology of the hypothetical NMOS input protection device is shown in figure 46. All metal connections are at

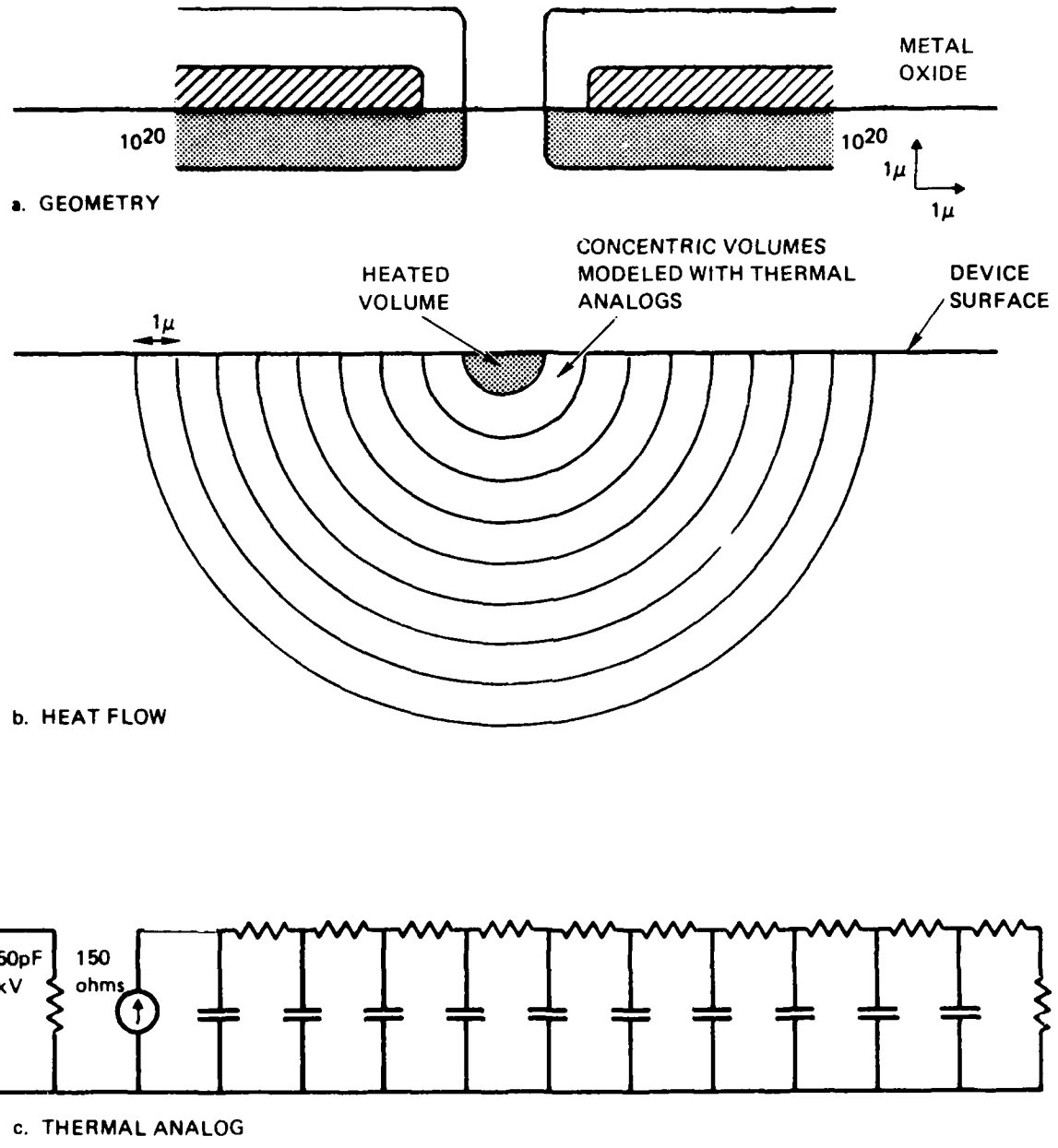


Figure 45. Thermal Model

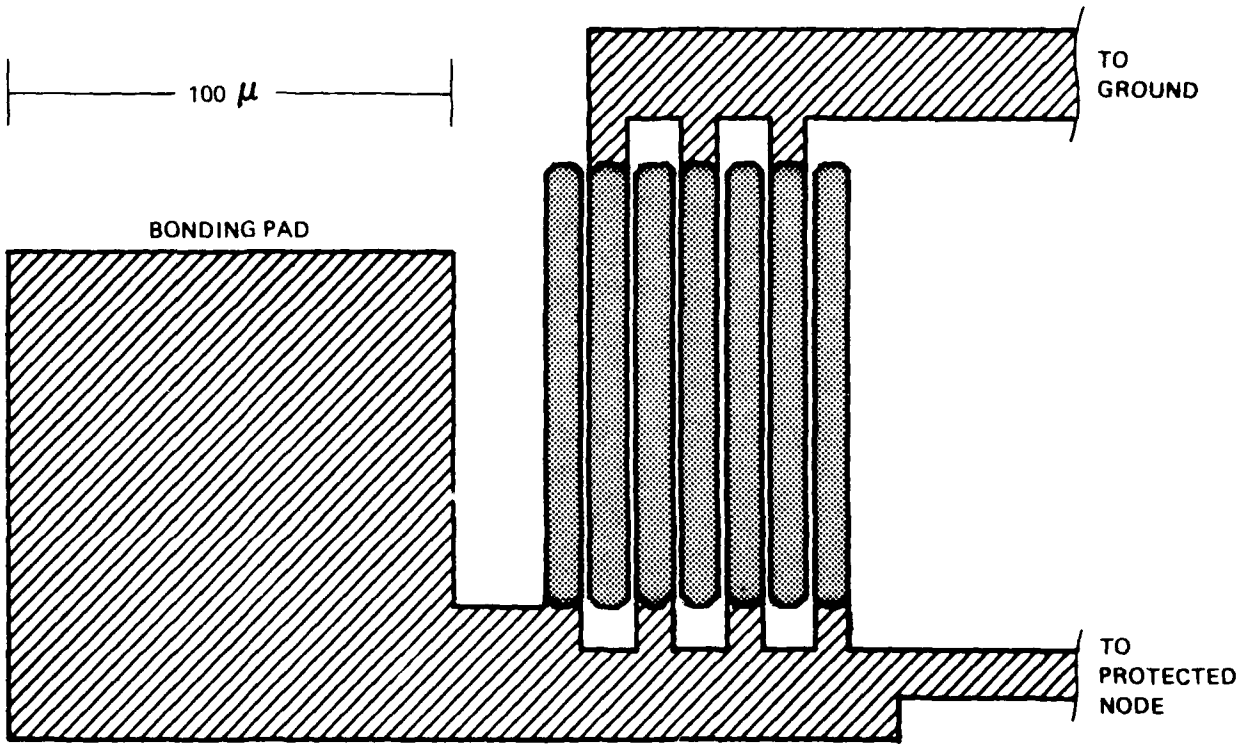


Figure 46. Protection Network for NMOS Technology

least 17 microns wide to avoid metallization failure. The corners of the protection network are rounded to avoid excessive fields in this region.

Two methods of implementing the protection network are possible. The first is to separate the N+ diffusions by a gate which would allow closely spaced diffusions as part of the self-aligned gate technology. A disadvantage of this approach is the need for a long length of thin oxide which must be defect free. An alternative is to separate the diffusions by a narrow strip of field oxide. The channel stop implantation under the field oxide would serve to lower the breakdown voltage at the surface. The advantage of this implementation is that thin oxide would not be required, thereby increasing the ESD hardness of the protection network.

The parasitic capacitance of this network may be estimated by calculating the capacitance from the diffusion to substrate and adding the capacitance from the diffusion to the heavily doped surface. Assuming a diffusion width of 10 microns, the diffusion to substrate capacitance is about $1x10^4$ pF/cm^2. For a structure 1,000 microns long, the total capacitance is 1 pF. The sidewall capacitance is about an order of magnitude higher per unit area. For 0.25-micron diffusion depths, the sidewall capacitance will be about 0.25 pF. The total capacitance is 1.25 pF which is not prohibitive.

In summary, avalanche injection offers the possibility of a low impedance shunt element. Current constrictions may be reduced by minimizing the initiating voltage. The initiating voltage may be reduced by increasing the surface P+ doping. Voltage drops across the conductivity modulated bulk region are minimized by close spacing between the N+ diffusions.

Since high stress conditions readily initiate avalanche injection, many existing input protection networks may owe their effectiveness to this mode of conduction. By optimizing the design of an avalanche injection device, improvements in the effectiveness of an input protection network may be obtained. High substrate doping and close spacing are inherent in the submicron process. Therefore, the possibility exists of using the characteristics of a submicron process to optimize an effective protection network based on avalanche injection.

SECTION IX
CONCLUSIONS AND RECOMMENDATIONS

The objective of this program was to investigate the EOS sensitivity of micron and submicron linewidth circuit structures and investigate improved EOS protection schemes. To achieve this, an attempt was made to design input protection networks which would protect a baseline submicron transistor, fabricated from a baseline submicron process, against baseline ESD threats. The design process included an examination of the features of existing input protection networks, a study of the factors which limit the ESD hardness of protection networks, and consideration of alternate approaches to achieve ESD hardness. The factors expected to determine the electrical overstress sensitivity of micron and submicron design rule microcircuit technologies were investigated through the use of computer-aided modeling techniques supported by an analytical effort.

Two candidate submicron technologies were considered in this study, CMOS and NMOS. The CMOS process allows greater design flexibility which is reflected in existing input protection networks which are highly effective. One input protection network for CMOS was described as being capable of withstanding a 4500-volt ESD which exceeded this program's design goal.

Compared to CMOS, existing input protection networks for NMOS devices are relatively ineffective. This is due largely to the limited design flexibility inherent in the NMOS process. Therefore, the program effort was directed toward integrated circuits fabricated using NMOS technology.

Series impedance elements were rejected for input protection networks because a series resistor large enough to have much effect on the ESD current would induce a voltage across the resistor sufficient to threaten the field oxide. Thus, the effort shifted to the design of a low impedance shunt element.

Conventional shunt elements such as zener or punch-through diodes proved to have series resistance much too high for adequate protection.

A mode of current conduction which seems to offer impedances low enough to be attractive is avalanche injection. Unfortunately, avalanche injection is characterized by current controlled negative resistance which tends to constrict current flow to a narrow, intensely heated region. However, by fabricating the device in a manner such that the initiating voltage for avalanche injection is approximately equal to the sustaining voltage, a device can be fabricated which will distribute current uniformly across its length. Such devices can be fabricated as part of the submicron NMOS process. Fabrication and ESD testing of this protection network is recommended.

The study was hampered by a lack of information on the physics and behavior of microplasmas. Analytical expressions describing the voltage drop across the avalanching region, the resistivity of the conductivity modulated region, and the geometry of microplasmas were found to be lacking. Since avalanche injection is such an important mode of conduction in devices exposed to electrical overstress and is the basis of the proposed NMOS protection network, additional research in this area could prove useful.

The versatility and effectiveness of computer-aided modeling techniques were demonstrated during this program. Electrical component analogs of thermal parameters allowed investigation of devices with nonlinear characteristics and complex geometries. A logical extension of the modeling effort is to develop electrical analogs of the electronic behavior of semiconductors. An existing lumped element model of semiconductors is the Linvill lumped model. Unfortunately, few network analysis codes contain Linvill lumped elements. A time domain network analysis program for microcomputers which included the capability of modeling the electronic behavior of semiconductors would be useful in modeling semiconductor behavior.

A potential trade-off exists between the amount of protection provided by an input protection network and its impacts on yield and reliability. An effective protection network, especially in NMOS, requires a large amount of contact area between the metallization and the N+

diffusions. But, a large amount of contact area enhances the probability of alloying spikes shorting through the N+ diffusion to the substrate. Such alloying spikes reduce circuit yield, and partial spikes may impact field reliability. Thus, one of the design rules in NMOS is to minimize metallization contact area. Of course, this is counter to the goal of minimizing shunt impedance in the protection network. It is necessary to trade-off the size of the protection network, hence, its degree of protection, against the yield and reliability impacts of large contact area. This trade-off is beyond the scope of the present effort, but it is recommended that such a trade-off be performed. The use of an interlevel conductor such as polysilicon between the aluminum and silicon could raise the failure level by resisting the formation of alloy spikes. It may be desirable to reduce the ESD specification below 4,000 V in the interests of improving yield and reliability.

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SYMBOLS

V	voltage
C	capacitance
E	energy
Vbd	breakdown voltage
N	doping concentration
Rs	spreading resistance
ρ	resistivity
d	diameter
W_d	width of the depletion region
ε_s	permittivity of silicon
V_{SL}	saturated velocity of elctrons and holes
A	area
I	current
W	device width
Q	charge
Tox	oxide thickness
Ids	drain to source current
L	device length
S	specific heat
P	thermal resistivity
q	electronic charge
u	mobility
n	electron concentration
p	hole concentration
N_D	donor dopant concentration
N_A	acceptor dopant concentration
n_i	intrinsic carrier concentration
T	temperature in degrees Kelvin
τ	minority carrier lifetime
x	distance from the junction
J	current density
Vgs	gate to substrate voltage
Vt	threshold voltage
α	ionization coefficient
k	Boltzmann's constant

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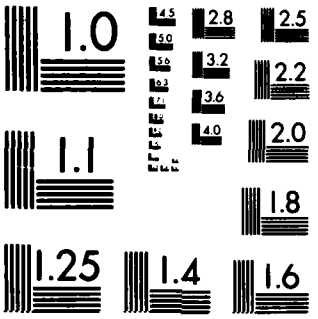
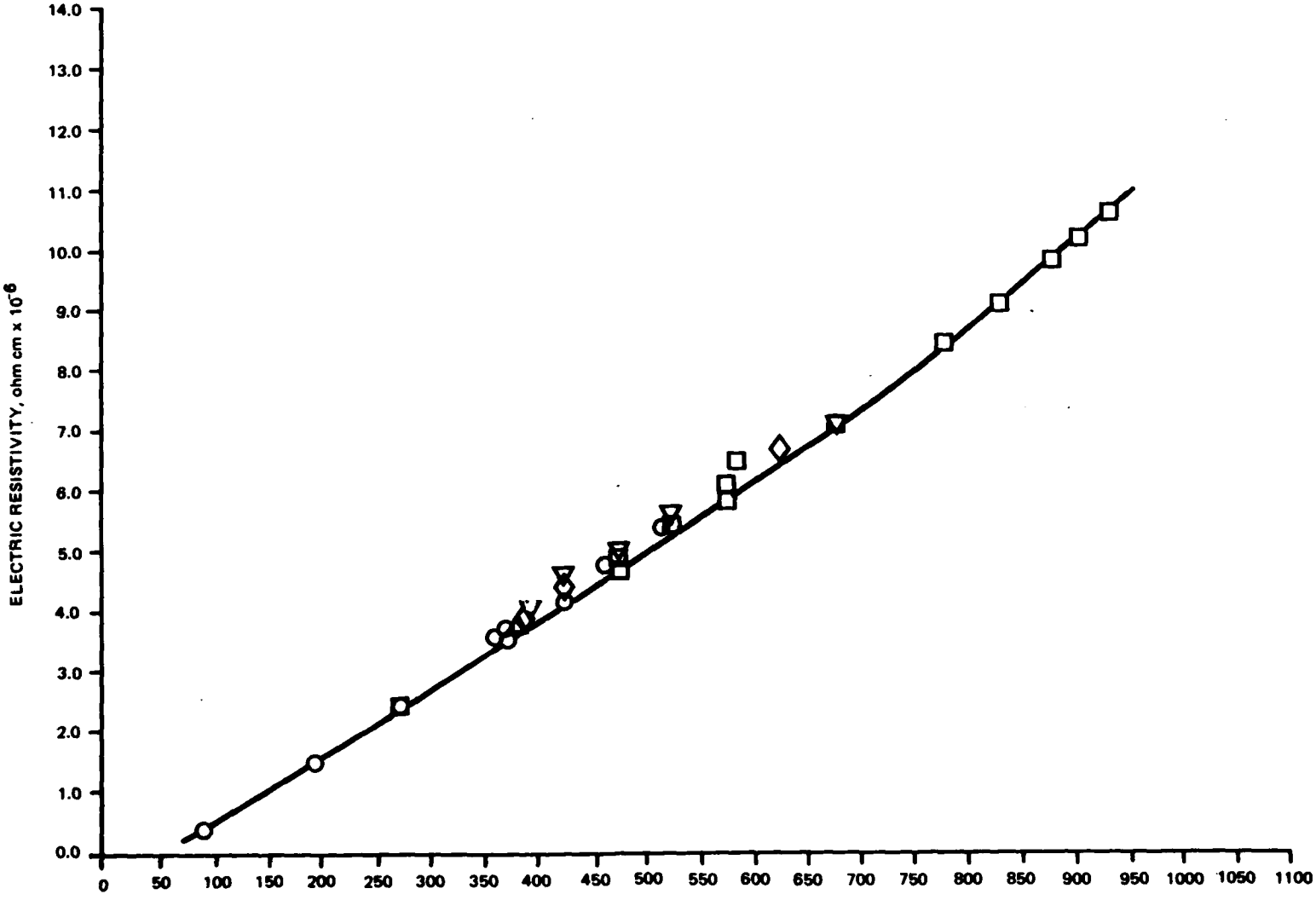
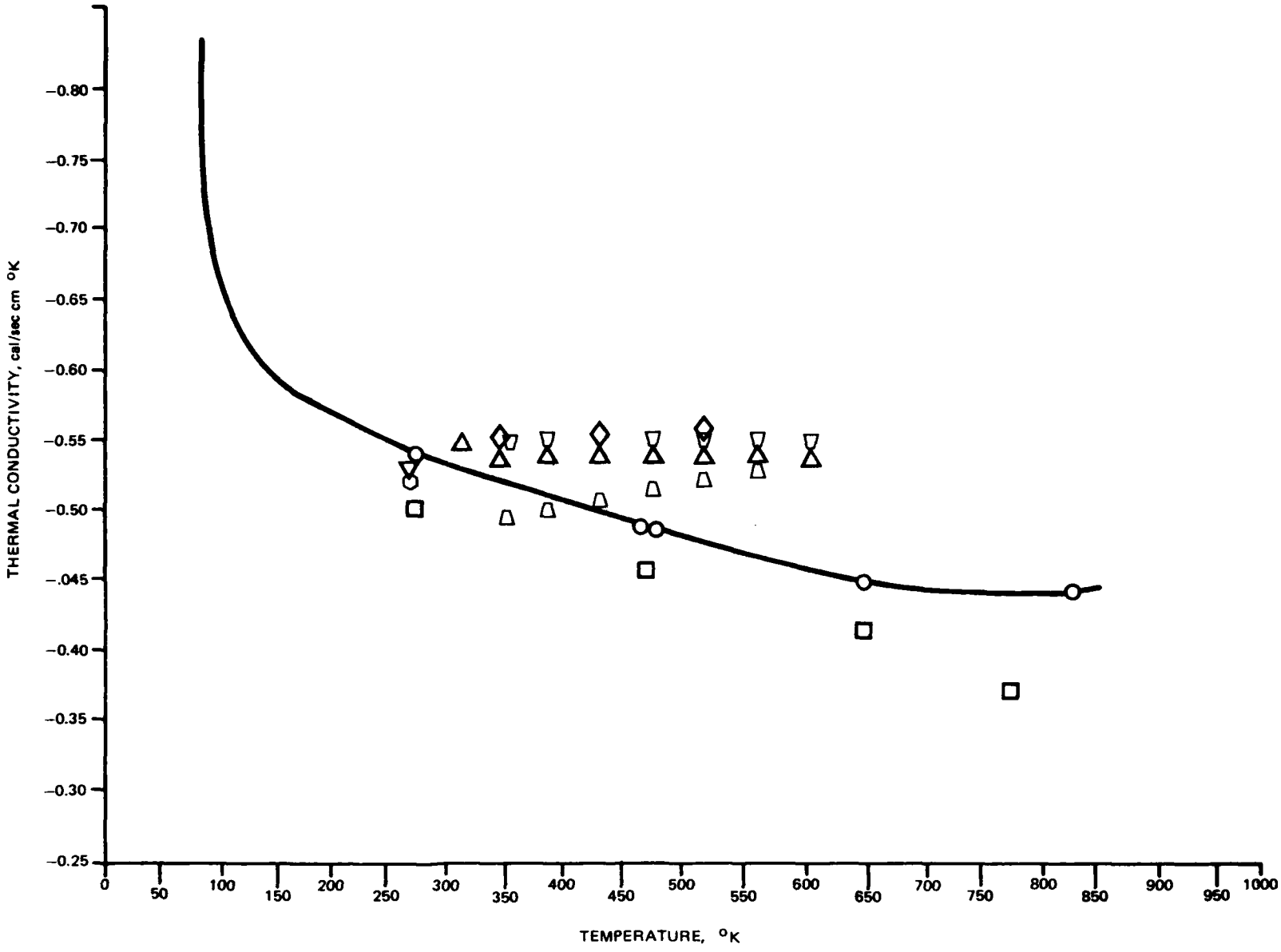


APPENDIX A

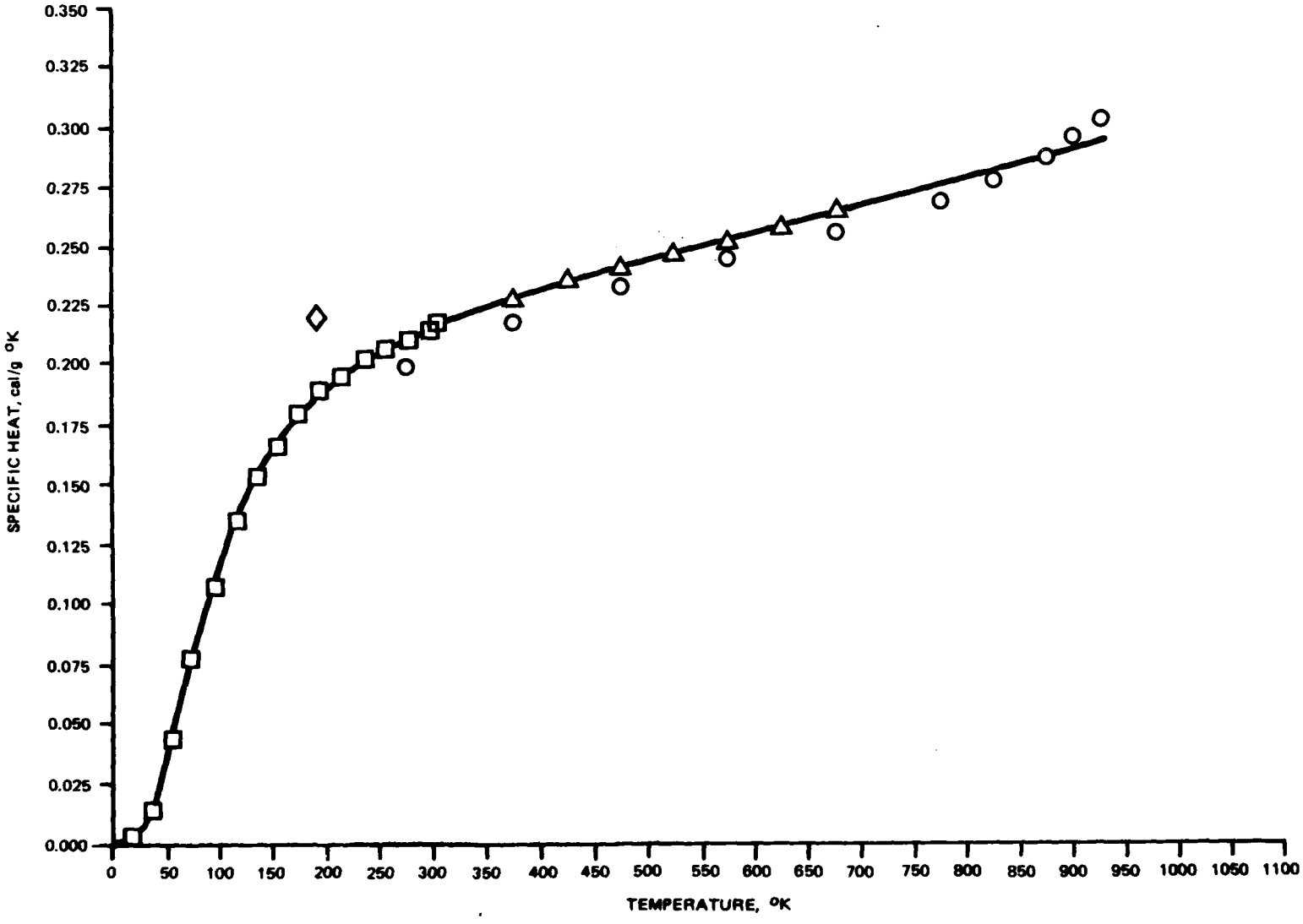
PROPERTIES OF MATERIALS



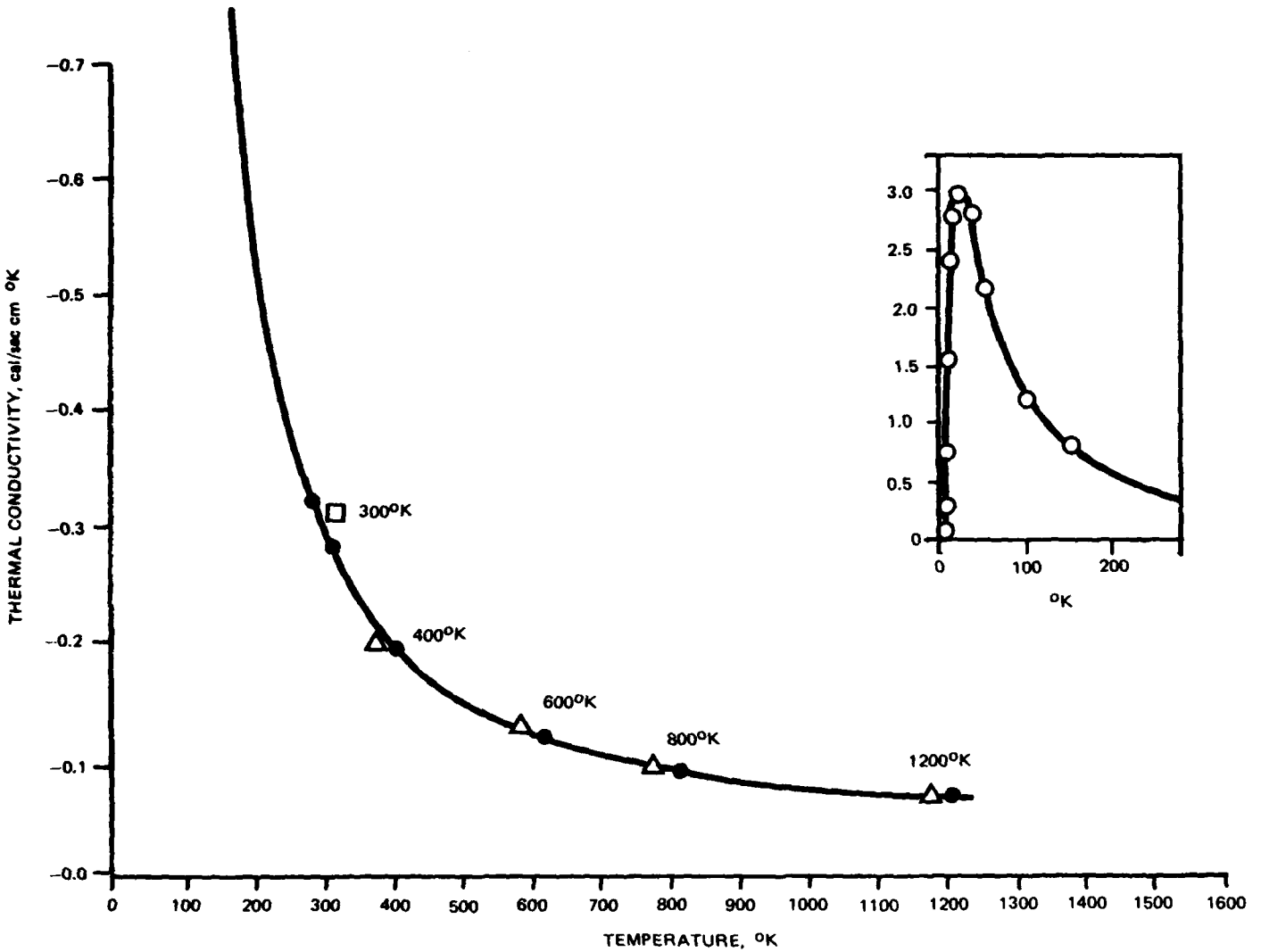
ELECTRIC RESISTIVITY – – ALUMINUM



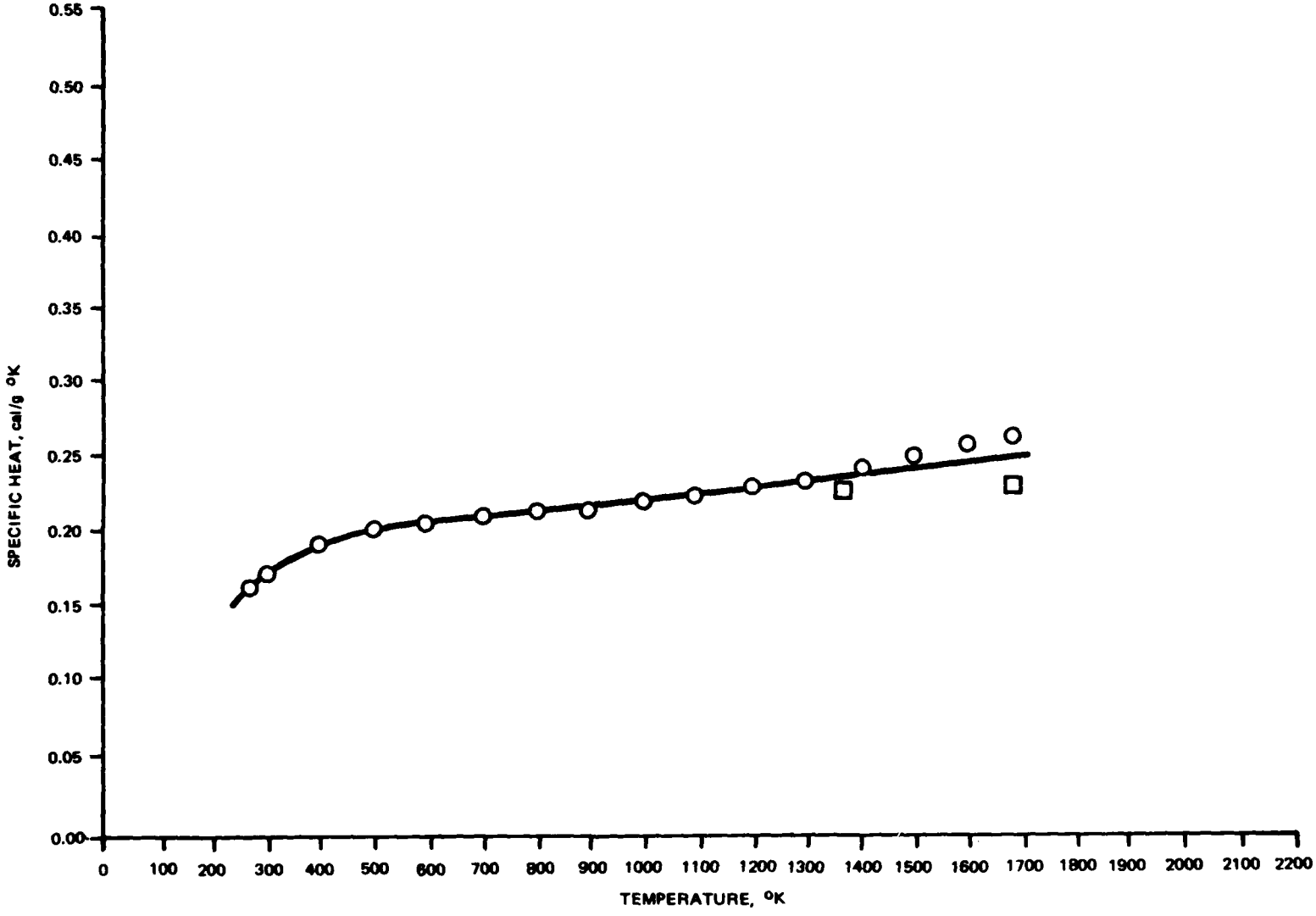
THERMAL CONDUCTIVITY – – ALUMINUM



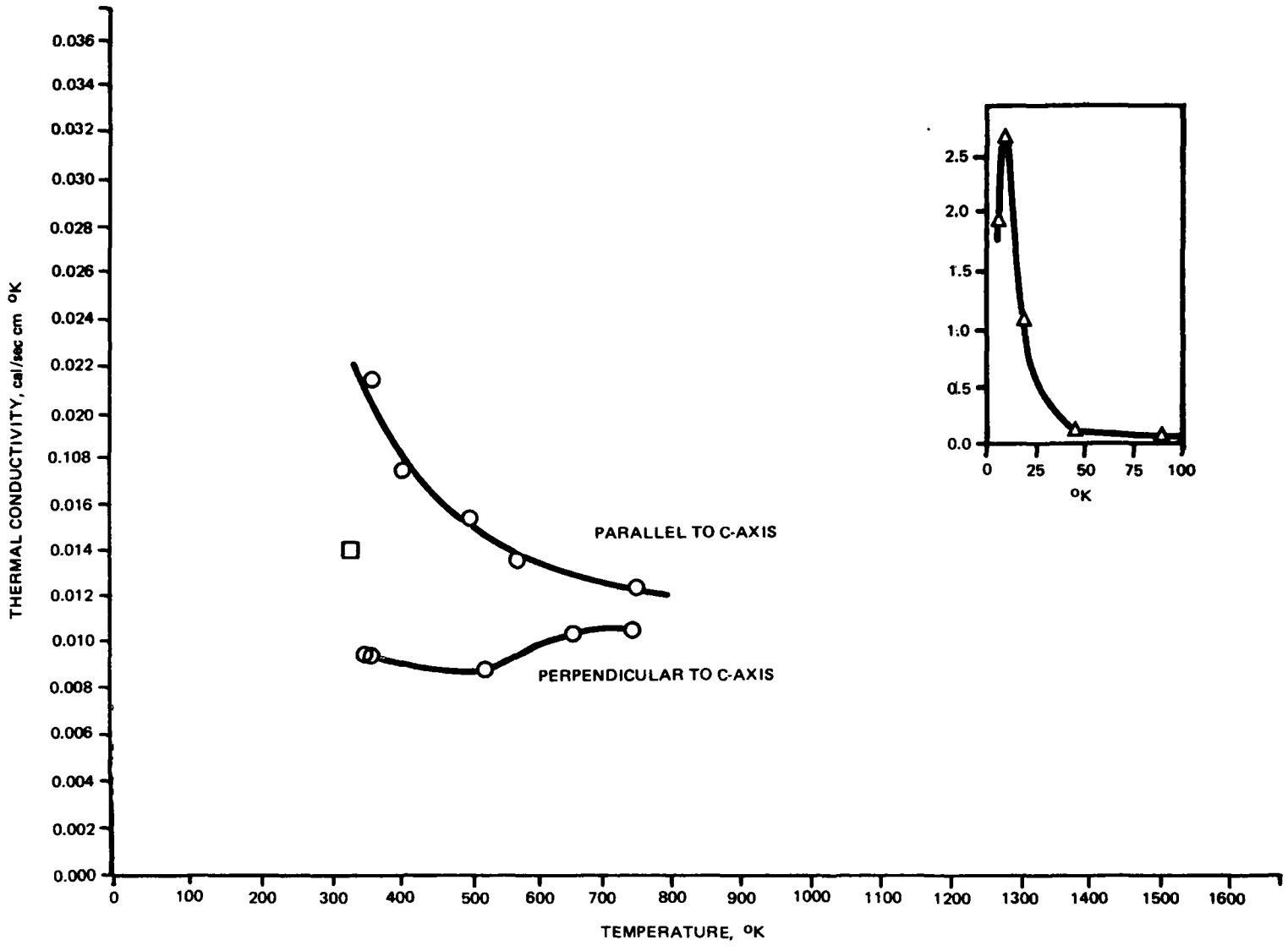
SPECIFIC HEAT – – ALUMINUM



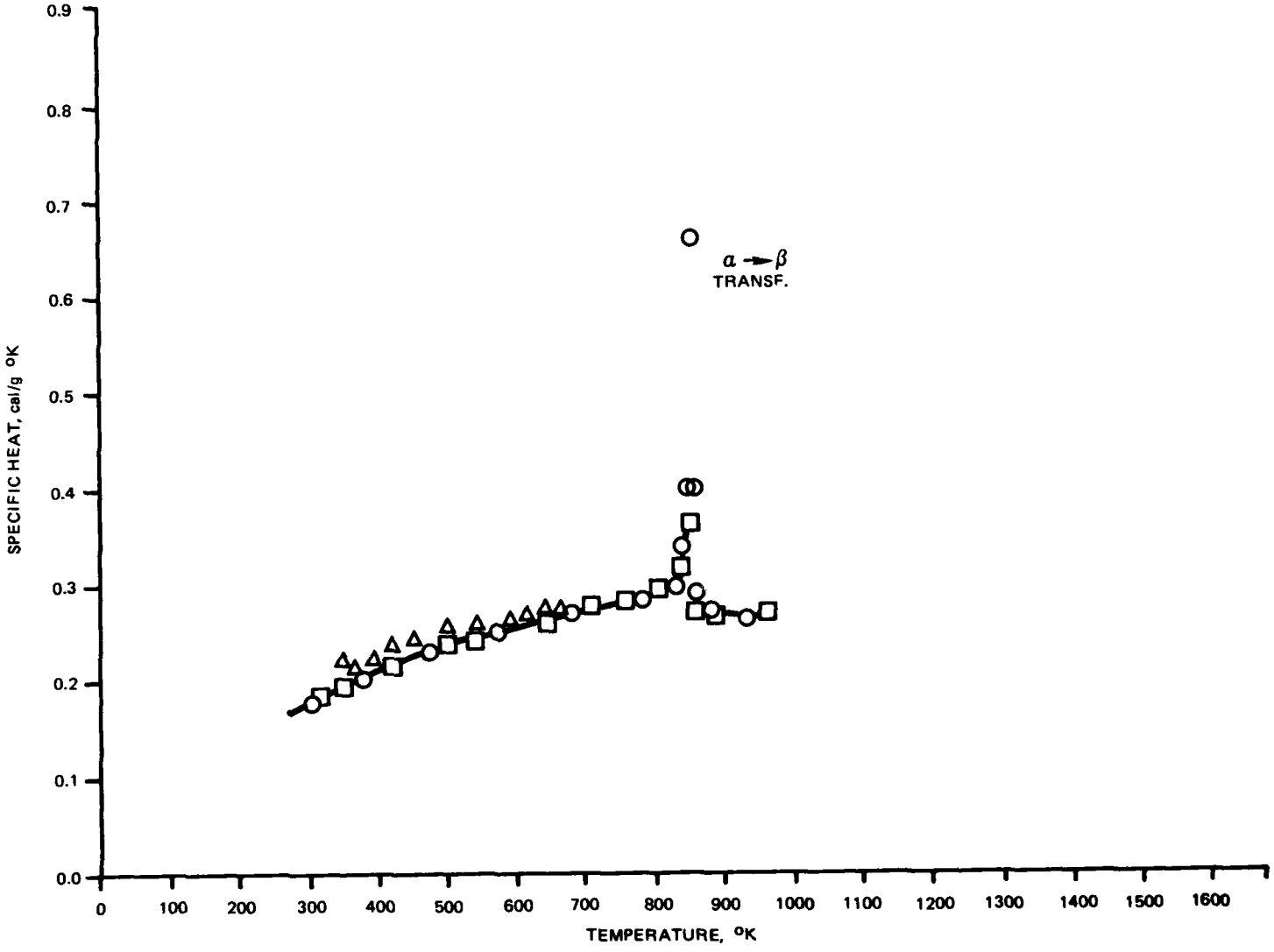
THERMAL CONDUCTIVITY -- SILICON



SPECIFIC HEAT – – SILICON



THERMAL CONDUCTIVITY -- SILICON OXIDE



SPECIFIC HEAT -- SILICON OXIDE

APPENDIX B

TIME DOMAIN NETWORK SIMULATION FOR MICROCOMPUTERS

Many of the simulation runs described in this report were made using simple time domain network analysis programs run on microcomputers. The network analysis codes utilized on the microcomputers were simple BASIC programs. The advantage of using a simple code was the high degree of freedom to modify the code to achieve a specific purpose. For example, the nonlinear dependence of the thermal resistance of silicon was treated by making the analagous resistor a function of the appropriate node voltage by simply modifying a line of the program. Modeling the same nonlinear dependence on most mainframe network analysis codes varies from difficult to impossible. Two sample programs are described in this appendix.

The network analysis codes utilized are based on the solution of the node equations. The node equations are an expression of Kirchoff's current law for each circuit node.

The node equations may be expressed in scalar form as:

$$\begin{bmatrix} y11 & y12 & \dots & y1n \\ y21 & y22 & \dots & y2n \\ & & & \\ \dots & \dots & \dots & \dots \\ yn1 & yn2 & \dots & ynn \end{bmatrix} \begin{bmatrix} e1 \\ e2 \\ . \\ . \\ en \end{bmatrix} = \begin{bmatrix} is1 \\ is2 \\ . \\ . \\ isn \end{bmatrix}$$

where:

(1) yii is the sum of the conductances of all branches connected to node i; yii is called the self-admittance of node i.

(2) yik is the negative of the sum of the conductances of all branches connecting node i and node k; yik is called the mutual admittance between node i and node k.

(3) isk is the algebraic sum of all source currents entering node k; the current sources entering node k are assigned a positive value.

(4) The yik elements make up the nodal admittance matrix, the ei and isi elements are the node voltage vector and the source current vector, respectively.

In vector notation, the node equations may be expressed as:

$$YnE = Is$$

Program TDA (Time Domain Analysis) assembles the nodal admittance matrix by taking each element, and summing the element conductance and source current to the appropriate matrix elements. The simultaneous node equations are then solved by Gaussian elimination.

TDA has built-in models for resistors, capacitors, inductors, current sources, voltage controlled current sources and diodes. Capacitors, inductors, and active devices can be modeled as voltage sources, current sources, or as a hybrid source. For example, the equations which describe the capacitor as a voltage source and a current source are:

$$V = \frac{1}{C} \int I dt \quad \rightarrow \quad V = \frac{1}{C} \sum I \Delta t$$

$$I = C \frac{dV}{dt} \quad \rightarrow \quad I = C \frac{\Delta V}{\Delta t}$$

Over the interval of one time step, the voltage source representation for the capacitor can be modified to a conductance representation by dividing both sides of the equation by current as follows:

$$G = \frac{C}{\Delta T}$$

After each time step, the capacitor is in equilibrium with its node voltages. This equilibrium can be modeled by placing a current source in parallel with the capacitor conductance with a value which will exactly oppose the current flow through the conductance after a time step. The advantage of representing the capacitor as a Norton source is improved

stability. The improved stability results by allowing the capacitor to respond during the time step as opposed to a response which lags by one time step.

Voltage and current representations for the inductor are:

$$V = L \frac{dI}{dt} \rightarrow V = L \frac{\Delta I}{\Delta t}$$

$$I = \frac{1}{L} \int V dt \rightarrow I = \frac{1}{L} \sum V \Delta t$$

Over the interval of one time step, the inductor can be represented as a conductance by modifying the current representation:

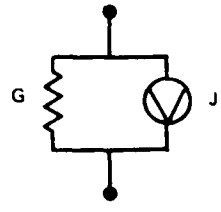
$$G = \frac{\Delta t}{L}$$

The build-up of current in the inductor is modeled by placing a current source in parallel with the inductor which sums the current flowing through the conductance following each time step. The Norton representation of the inductor yields improved stability since the inductor responds during each time step instead of lagging by one time step.

A summary of the Norton source representation of the allowable elements of the TDA code follows:

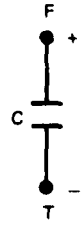
RESISTOR

G = 1/R
J = 0



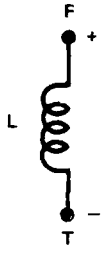
CAPACITOR

G = C/ΔT
–J = Δ VC/ΔT



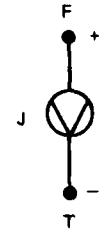
INDUCTOR

$G = \Delta T/L$
$J = J + \Delta V \Delta T/L$



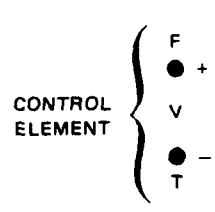
CURRENT SOURCE

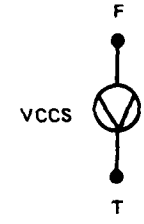
$G = 0$
$J = J$



VOLTAGE CONTROLLED CURRENT SOURCE

$G = 0$
$J = Vgm$



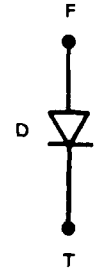


DIODE

$G = 1$ (FORWARD BIAS)
$J = 0$

$G = 1/1 \times 10^{6}$ (REVERSE BIAS)
$J = 0$

$G = 1/Rs$ (BREAKDOWN)
$J = Vbd/Rs$



A drawback of a simultaneous solution of the node equations is the memory required to store the nodal admittance matrix, roughly n^2 locations, and the number of operations required for Gaussian elimination, roughly $n^{3/3}$. For a circuit with 200 nodes, 40000 memory locations are

required for the nodal admittance matrix, and 2.7×10^6 operations are required to solve the network.

An alternative method of solving the node equations is by iteration. For large networks, iteration is faster and uses less memory than a direct solution.

Program iTDA (iterative Time Domain Analysis) was developed to solve networks using Gauss-Seidel Iteration. The basic method is to cyclically and repetitively solve the node equations for en. For example, the node equation for V_0 in the circuit of figure B-1 is a function of V_1-V_4 and Y_1-Y_4. The voltage of V_0 which satisfies Kirchoff's current law is:

$$V_0 = \frac{\sum Vn\ Yn}{\sum Yn}$$

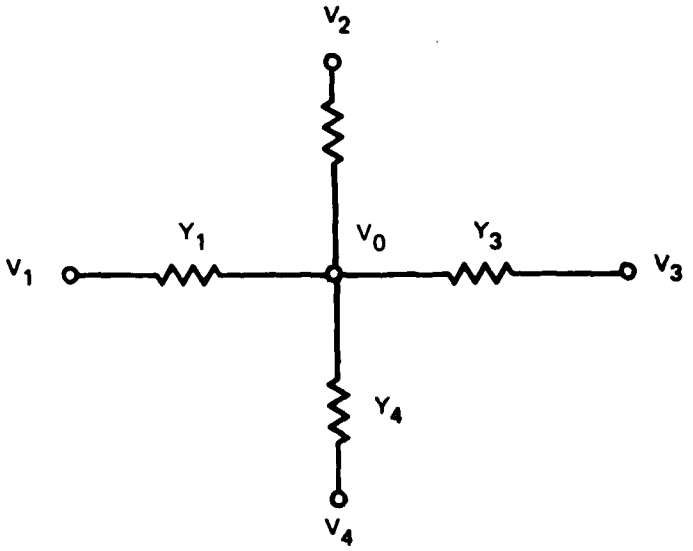


Figure B-1. Example Network Node

Each iteration yields a more accurate value for the node voltages. The iTDA program iterates each node voltage once during each time step.

An important consideration when using iteration is the rate of convergence. Qualitatively, the rate of convergence seems to depend on

the uniformity of the network. For example, iteration will converge faster for a resistor chain network when all the resistors have similar values than when the resistors have extreme differences in values. Since materials problems tend to have uniform networks, iteration is efficient and practical.

TDA and iTDA always use node zero as the datum or ground node. The maximum number of nodes does not include the datum node. Nodes must be numbered in a continuous numeric sequence starting from one. The order in which nodes are numbered is not important for TDA and has only a small effect for iTDA.

The listing for program TDA is given in figure B-2. The listing for program iTDA is given in figure B-3. The potential user should note that these simple codes do not have many of the capabilities and protection built into complex mainframe circuit analysis codes. It is the responsibility of the user to ensure that these codes are applicable to the problem and that the results are reasonable.

```
10   Program TDA (Time Domain Analysis)
20   Written by Phillip Young, BDM Corp. 1984
30 '
40 '
50 DIM TY(50),F(50),T(50),Z(50),V(50),Y(50,50),I(50),CE(50)
60 CLS
70 '
80 '
90 GOSUB 240                          'input
100 GOSUB 490                         'initialize y-matrix
110 FOR C=1 TO CO                     'sum components of y-matrix for each element
120 IF TY(C)=1 THEN GOSUB 560         'resistor
130 IF TY(C)=2 THEN GOSUB 620         'capacitor
140 IF TY(C)=3 THEN GOSUB 710         'inductor
150 IF TY(C)=4 THEN GOSUB 800         'current source
160 IF TY(C)=5 THEN GOSUB 840         'diode
170 IF TY(C)=6 THEN GOSUB 930         'voltage controlled current source
180 NEXT C                            'end loop
190 GOSUB 990                         'solve y-matrix by gaussian elimination
200 PRINT T;V(N1)                     'print output
210 T=T+TO                            'increment time
220 IF T<T9 THEN 100                   check for stoptime
230 END
240 PRINT "input q,q..."
250 PRINT "1. no. of elements"
260 PRINT "2. no. of nodes"
270 PRINT "3. output node"
280 PRINT "4. stop time"
290 PRINT "5. step size"
300 INPUT CO,NO,N1,T9,TO
310 FOR C=1 TO CO
320 PRINT "input element, from, to, value"
330 INPUT A$,F(C),T(C),Z(C)
340 IF A$="r" THEN TY(C)=1
350 IF A$="c" THEN TY(C)=2
360 IF A$="l" THEN TY(C)=3
370 IF A$="j" THEN TY(C)=4
380 IF A$="vccs" THEN GOSUB 1160
390 IF A$="d" THEN GOSUB 1200
400 NEXT C
410 T=0
420 FOR N=1 TO NO
430 V(N)=0
440 NEXT N
450 FOR N=1 TO CO
460 I(N)=0
470 NEXT N
480 RETURN
490 FOR I=1 TO NO
500 FOR J=1 TO NO+1
510 Y(I,J)=0
520 NEXT J
530 NEXT I
540 RETURN
550 FOR C=1 TO CO
560 'resistor
570 Y(F(C),T(C))=Y(F(C),T(C))-1/Z(C)
580 Y(T(C),F(C))=Y(T(C),F(C))-1/Z(C)
590 Y(F(C),F(C))=Y(F(C),F(C))+1/Z(C)
600 Y(T(C),T(C))=Y(T(C),T(C))+1/Z(C)
610 RETURN
```

Figure B-2. Program TDA Listing

```
620  capacitor
630 Y(F(C),T(C))=Y(F(C),T(C))-Z(C)/TO
640 Y(T(C),F(C))=Y(T(C),F(C))-Z(C)/TO
650 Y(F(C),F(C))=Y(F(C),F(C))+Z(C)/TO
660 Y(T(C),T(C))=Y(T(C),T(C))+Z(C)/TO
670 I(C)=(V(T(C))-V(F(C)))*Z(C)/TO
680 Y(F(C),NO+1)=Y(F(C),NO+1)-I(C)
690 Y(T(C),NO+1)=Y(T(C),NO+1)+I(C)
700 RETURN
710 'inductor
720 Y(F(C),T(C))=Y(F(C),T(C))-TO/Z(C)
730 Y(T(C),F(C))=Y(T(C),F(C))-TO/Z(C)
740 Y(F(C),F(C))=Y(F(C),F(C))+TO/Z(C)
750 Y(T(C),T(C))=Y(T(C),T(C))+TO/Z(C)
760 I(C)=I(C)+(V(F(C))-V(T(C)))*TO/Z(C)
770 Y(F(C),NO+1)=Y(F(C),NO+1)-I(C)
780 Y(T(C),NO+1)=Y(T(C),NO+1)+I(C)
790 RETURN
800 'current source
810 Y(F(C),NO+1)=Y(F(C),NO+1)-Z(C)
820 Y(T(C),NO+1)=Y(T(C),NO+1)+Z(C)
830 RETURN
840 'diode
850 VD=V(F(C))-V(T(C))
860 IF VD>=0 THEN Z(C)=1
870 IF VD<0 AND VD>=-VB(C) THEN Z(C)=1000000!
880 IF VD>=-VB(C) THEN 920
890 Z(C)=RS(C)
900 Y(F(C),NO+1)=Y(F(C),NO+1)-VB(C)/RS(C)
910 Y(T(C),NO+1)=Y(T(C),NO+1)+VB(C)/RS(C)
920 GOTO 570
930 'voltage controlled current source
940 Y(F(C),F(CE(C)))=Y(F(C),F(CE(C)))-Z(C)
950 Y(F(C),T(CE(C)))=Y(F(C),T(CE(C)))+Z(C)
960 Y(T(C),F(CE(C)))=Y(T(C),F(CE(C)))-Z(C)
970 Y(T(C),T(CE(C)))=Y(T(C),T(CE(C)))+Z(C)
980 RETURN
990 'gausssian elimination routine
1000 FOR K=1 TO NO
1010 FOR I=1 TO NO
1020 IF Y(I,K)=0 THEN 1100
1030 AA=Y(I,K)/Y(K,K)
1040 AB=Y(K,K)
1050 FOR J=1 TO NO+1
1060 IF Y(K,J)=0 THEN 1090
1070 IF K<>I THEN Y(I,J)=Y(I,J)-AA*Y(K,J)
1080 IF K=I THEN Y(I,J)=Y(I,J)/AB
1090 NEXT J
1100 NEXT I
1110 NEXT K
1120 FOR K=1 TO NO
1130 V(K)=Y(K,NO+1)
1140 NEXT K
1150 RETURN
1160 TY(C)=6
1170 PRINT "input control element number"
1180 INPUT CE(C)
1190 RETURN
1200 PRINT "input breakdown voltage, zener resistance"
1210 INPUT VB(C),RS(C)
1220 TY(C)=5
1230 RETURN
```

Figure B-2. Program TDA Listing (Concluded)

```
10 ' Program iTDA (iterative Time Domain Analysis)
20 ' Written by Phillip Young, BDM Corp. 1984
30 '
40 '
50 DIM TY(50),F(50),T(50),Z(50),V(50),I(50),CE(50)
60 CLS
70 '
80 '
90 GOSUB 350                        'input
100 FOR N=1 TO NO                   'find all elements connected to node N
110 A=0                             'initialize A
120 B=0                             'initialize B
130 FOR C=1 TO CO                   'check each element for connection to N
140 IF F(C)<>N THEN 190             'check from node of element c
150 IF TY(C)=1 THEN GOSUB 580       'resistor
160 IF TY(C)=2 THEN GOSUB 620       'capacitor
170 IF TY(C)=3 THEN GOSUB 660       'inductor
180 IF TY(C)=4 THEN GOSUB 700       'current source
190 IF T(C)<>N THEN 240             'check to node of element c
200 IF TY(C)=1 THEN GOSUB 730       'resistor
210 IF TY(C)=2 THEN GOSUB 770       'capacitor
220 IF TY(C)=3 THEN GOSUB 810       'inductor
230 IF TY(C)=4 THEN GOSUB 850       'current source
240 NEXT C                          'check next element
250 V(N)=A/B                        'calculate voltage of node n
260 NEXT N                          'do next node
270 FOR C=1 TO CO                                                   'calc currents
280 IF TY(C)=2 THEN I(C)=(V(F(C))-V(T(C)))*Z(C)/TO                  'for capacitors
290 IF TY(C)=3 THEN I(C)=I(C)+(V(T(C))-V(F(C)))*TO/Z(C)             'for inductors
300 NEXT C                                                          'next element
310 PRINT T;V(N1)                   'output
320 T=T+TO                          'increment time
330 IF T<T9 THEN 100                'check for stoptime
340 END
350 PRINT "input q,q..."
360 PRINT "1. no. of elements"
370 PRINT "2. no. of nodes"
380 PRINT "3. output node"
390 PRINT "4. stop time"
400 PRINT "5. step size"
410 INPUT CO,NO,N1,T9,TO
420 FOR C=1 TO CO
430 PRINT "input element, from, to, value"
440 INPUT A$,F(C),T(C),Z(C)
450 IF A$="r" THEN TY(C)=1
460 IF A$="c" THEN TY(C)=2
470 IF A$="l" THEN TY(C)=3
480 IF A$="j" THEN TY(C)=4
490 NEXT C
500 T=0
510 FOR N=0 TO NO
520 V(N)=0
530 NEXT N
540 FOR N=1 TO CO
550 I(N)=0
560 NEXT N
570 RETURN
580 'resistor
590 A=A+V(T(C))/Z(C)
600 B=B+1/Z(C)
610 RETURN
```

Figure B-3. Program iTDA Listing

```
620 'capacitor
630 A=A+I(C)+V(T(C))*Z(C)/TO
640 B=B+Z(C)/TO
650 RETURN
660 'inductor
670 A=A+I(C)+V(T(C))*TO/Z(C)
680 B=B+TO/Z(C)
690 RETURN
700 'current source
710 A=A-Z(C)
720 RETURN
730 'resistor
740 A=A+V(F(C))/Z(C)
750 B=B+1/Z(C)
760 RETURN
770 'capacitor
780 A=A-I(C)+V(F(C))*Z(C)/TO
790 B=B+Z(C)/TO
800 RETURN
810 'inductor
820 A=A-I(C)+V(F(C))*TO/Z(C)
830 B=B+TO/Z(C)
840 RETURN
850 'current source
860 A=A+Z(C)
870 RETURN
```

Figure B-3. Program iTDA Listing (Concluded)

APPENDIX C

BIBLIOGRAPHY

The literature search was updated for the period since 1977 when our last literature search in this area was performed for RADC. The literature was divided into four areas: Pulsed EOS Testing, Human Body EOS, Device Charge-Discharge EOS, and RF EOS. Each of these areas is discussed in the following sections.

A. PULSED EOS TESTING

The literature on pulsed EOS testing was searched to determine whether any data could be found to support this research. The references found were:

Pancholy, R. K. (Rockwell International, Anaheim, CA). GATE PROTECTION FOR CMOS/SOS. IEEE - 15th Reliability Physics Symposium, Catalogue No. 77CH1195-7PHY, April 1977, pp. 132-137.

Pease, R. L., D. R. Alexander, and C. R. Jenkins, (BDM Corp., Albuquerque, NM). ELECTRICAL OVERSTRESS TEST PROGRAM AND INTEGRATED CIRCUIT FAILURE MODE EVALUATION. Rept. No. DNA 4467F, Contract No. DNA 001-77-C-0156, Subtask 299QAXTB097-04, April 26, 1978, 108 pp.

Alexander, D. R. (Sandia National Laboratories, Albuquerque, NM) E. W. Enlow, and R. J. Karaskiewicz (BDM Corp., Albuquerque, NM). FAILURE THRESHOLD DISTRIBUTIONS IN BIPOLAR TRANSISTORS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 59-66.

Formanek, V. C. (IIT Research Institute, Chicago, IL). DAMAGE RESPONSE OF SELECTED INTERFACE INTEGRATED CIRCUITS TO A SIMULATED EMP WAVEFORM. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 158-167.

Whalen, J. J. (SUNY at Buffalo, Amherst, NY) and H. Domingos (Clarkson College of Technology, Potsdam, NY). SQUARE PULSE AND RF PULSE OVERSTRESSING OF UHF TRANSISTORS. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, 7 pp.

Young, P. A., R. J. Karaskiewicz, (BDM Corp., Albuquerque, NM) and D. R. Alexander (Sandia National Laboratories, Albuquerque, NM). ELECTRICAL OVERSTRESS INVESTIGATIONS IN MODERN INTEGRATED CIRCUIT TECHNOLOGIES. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, Contract No. F29601-77-C-0099, pp. 114-119.

Denson, W. K., and K. A. Key (Reliability Analysis Center, Griffiss AFB, NY). VZAP TEST RESULTS OF THE 74F04 AND 74F175 DEVICES AND CORRELATION STUDY. Rept. No. 01115-20-3, December 14, 1981, 156 pp.

Most of these references cite work already known by BDM. Data contained in them has been noted for possible inclusion in this program.

B. HUMAN BODY MODEL FOR ESD

A large amount of literature was found on the subject of human body models for ESD and component testing using those models. The principal references are listed below.

Nakamura, T., H. Kunita, and H. Ihara (Nippon Electric Co., Ltd., Japan). ELECTROSTATIC DISCHARGE EFFECTS ON MOS MEMORY ICS. NEC Research and Development, No. 58, UDC 621.3.049.77: 537.24, July 1980, pp. 15-24.

Porter, D. C., R. D. Price, and L. K. Brooks (Boeing Co., Seattle, WA). EVALUATION OF PLASTIC LSI CIRCUITS. Rept. No. D180-22945-1, Contract No. DAAH01-76-C-0455, 56 pp.

Gallace, L. J., and H. L. Pujol (RCA/Solid State Division, Somerville, NJ). THE EVALUATION OF CMOS STATIC-CHARGE PROTECTION NETWORKS AND FAILURE MECHANISMS ASSOCIATED WITH OVERSTRESS CONDITIONS AS RELATED TO DEVICE LIFE. IEEE - 15th Reliability Physics Symposium, Las Vegas, Nevada, ST-6638, April 1977, 30 pp.

Antinone, R. J. (BDM Corp., Albuquerque, NM). SPECIFICATIONS FOR MICROCIRCUIT ELECTRICAL OVERSTRESS TOLERANCE, VOL. I. Rept. No. RADC-TR-78-28, Contract No. F30602-76-C-0308, March 1978, 139 pp.

Schreier, L. A. (Hughes Aircraft Company, Culver City, CA). ELECTROSTATIC DAMAGE SUSCEPTIBILITY OF SEMICONDUCTOR DEVICES. IEEE - 16th Reliability Physics Symposium, 1978, 7 pp.

Schwank, J. R., G. D. Jarrell, and M. G. Armendariz (Sandia National Laboratories). STUDY OF ELECTROSTATIC DISCHARGE EFFECTS ON COMMERCIAL CMOS DEVICES. Rept. No. SAND79-1784, February 1980, 47 pp.

Calvin, H., H. Hyatt, H. Mellberg, and D. Pellinen (Experimental Physics Corp., Hayward, CA). MEASUREMENT OF FAST TRANSIENTS AND APPLICATION TO HUMAN ESD. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 225-230.

Zajac, H. (Tektronix, Inc., Beaverton, OR). STUDY OF EFFECTS OF ELECTROSTATIC DISCHARGE ON SOLID-STATE DEVICES. National Electronic Packaging and Products Conference, Vol. I, 1980.

Keller, J. K. (Bell Laboratories, Allentown, PA). PROTECTION BY INTEGRATED CIRCUITS FROM DESTRUCTION BY ELECTROSTATIC DISCHARGE. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 73-80.

Castle, G. S. P., and D. R. Hibbert (University of Western Ontario, Faculty of Engineering Science, London, Ontario) and W. D. Greason (Northern Telecom, Canada Limited, London, Ontario). ANALYSIS OF ESD DAMAGE IN JFET PREAMPLIFIERS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 67-72.

Hart, A. R., and T. Teng (Hewlett Packard Co., Corvallis Division, Corvallis, OR). LSI DESIGN CONSIDERATIONS FOR ESD PROTECTION STRUCTURES RELATED TO PROCESS AND LAYOUT VARIATIONS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue EOS-2, September 9-11, 1980, pp. 87-94.

Turner, T. E., and S. Morris (Mostek Corp., Carrollton, TX). ELECTROSTATIC SENSITIVITY OF VARIOUS INPUT PROTECTION NETWORKS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 95-103.

Antinone, R. J. (The BDM Corp., Albuquerque, NM). MICROCIRCUIT ELECTRICAL OVERSTRESS TOLERANCE TESTING AND QUALIFICATION. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 184-188.

Goel, A. (American Microsystems, Inc., Santa Clara, CA). PROCEDURE FOR TESTING ELECTROSTATIC DISCHARGE SUSCEPTIBILITY OF MOS DEVICES. 19th Annual Reliability Physics Proceeding, Catalogue No. 81CH1619-6, April 7-9, 1981, pp. 200-203.

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Madzy, T. M., and L. A. Price, II (IBM Corp., Systems Products Division, Endicott, NY). MODULE ELECTROSTATIC DISCHARGE SIMULATOR. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 36-40.

Teng, T., A. R. Hart, and A. McKenna (Hewlett-Packard Co., Corvallis Division, Corvallis, OR). SUSCEPTIBILITY OF LSI MOD TO ELECTRO-STATIC DISCHARGE AT ELEVATED TEMPERATURE. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 168-175.

Mardiguian, A. E. (U.S. Air Force Weapons Laboratory, Kirtland AFB, NM). MICROCRACKS AND METALLIZATION BURNOUT. AFWL-TR-78-92, September 1979, 88 pp.

Anand, Y. (Microwave Associates, Inc., Burlington, MA) G. Morris, and V. Higgins (U.S. Army Electronics Technology and Device Laboratory, ERADCOM, Fort Monmouth, NJ). ELECTROSTATIC FAILURE OF X-BAND SILICON SCHOTTKY BARRIER DIODES. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 97-103.

Hyatt, H., H. Calvin, and H. Calvin, and H. Mellberg (Experimental Physics Corp., Hayward, CA). A CLOSER LOOK AT THE HUMAN ESD EVENT. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 1-8.

Hulett, T. V. (Microprocessor Design, Motorola Semiconductor Group, Austin, TX). ON-CHIP PROTECTION OF HIGH DENSITY NMOS DEVICES. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 90-96.

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McCullough, D. T., C. H. Lane, and R. A. Blore (U.S. Air Force, Rome Air Development Center, Griffiss AFB, NY). RELIABILITY OF EOS SCREENED GOLD DOPED 4002 CMOS DEVICES. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 36-40.

Branberg, G. (Hewlett-Packard Co., Loveland, CO). ELECTROSTATIC DISCHARGE AND CMOS LOGIC. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 55-63.

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King, W. M. (Electromagnetic Compatibility Advisor, Santa Monica, CA). DYNAMIC WAVEFORM CHARACTERISTICS OF PERSONNEL ELECTROSTATIC DISCHARGE. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 78-87.

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Japan). FAILURE ANALYSIS OF MICROCIRCUITS SUBJECTED TO ELECTRICAL OVERSTRESS. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 88-96.

Anand, Y. (Microwave Associates, Inc., Burlington, MA) G. Morris, and V. Higgins (U.S. Army Electronics Technology and Device Laboratory, ERADCOM, Fort Monmouth, NJ). ELECTROSTATIC FAILURE OF X-BAND SILICON SCHOTTKY BARRIER DIODES. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 97-103.

Moon, M. G. (Harris Semiconductor, Products Division, Melbourne, FL). ESD SUSCEPTIBILITIES OF HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 104-108.

Petrizio, C. J. (RCA Solid State Division, Somerville, NJ). ELECTRICAL OVERSTRESS VERSUS DEVICE GEOMETRY. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 183-187.

Minear, R. L., and G. A. Dodson (Bell Telephone Laboratories, Reading, PA). THE PHANTOM EMITTER - AN ESD - RESISTANT BIPOLAR TRANSISTOR DESIGN AND ITS APPLICATIONS TO LINEAR INTEGRATED CIRCUITS. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 188-192.

Castle, G. S. P., and D. R. Hibbert (University of Western Ontario, Faculty of Engineering Science, London, Ontario) and W. D. Greason (Northern Telecom, Canada Limited, London, Ontario). ANALYSIS OF ESD DAMAGE IN JFET PREAMPLIFIERS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 67-72.

Schwank, J. R., R. P. Baker, and M. G. Armendariz (Sandia National Laboratories, Albuquerque, NM). SURPRISING PATTERNS OF CMOS SUSCEPTIBILITY TO ESD AND IMPLICATIONS ON LONG-TERM RELIABILITY. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 104-111.

Taylor, R. (Mostek Corp., Carrollton, TX). INPUT PROTECTION DESIGN FOR THE 3u NMOS PROCESS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 97-100.

Head, G. O. (Lear Siegler, Inc., Instrument Division, Grand Rapids, MI). TIME-RELATED IMPROVEMENTS OF ELECTRICAL CHARACTERISTICS IN ELECTROSTATICALLY DAMAGE OPERATIONAL AMPLIFIERS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 225-228.

These papers and reports represent a number of techniques for testing of and hardening against the effects of ESD from humans. A great deal of discussion and controversy continues over how best to model the human body ESD event. Based on the search, we have modified our model as discussed in chapter II.

C. DEVICE CHARGE - DISCHARGE MODEL

Only three papers discussing this effect have been found. The first reference was the primary one used to establish our model.

Bossard, P. R., R. G. Chemelli, and B. A. Unger (Bell Laboratories, Murray Hill, NJ). ESD DAMAGE FROM TRIBOELECTRICALLY CHARGED IC PINS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-2, September 9-11, 1980, pp. 17-22.

Unger, B., R. Chemelli, P. Bossard, and M. Hudock (Bell Laboratories, Murray Hill, NJ). EVALUATION OF INTEGRATED CIRCUIT SHIPPING TUBES. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 57-64.

Chase, E. W. (Bell Laboratories, Murray Hill, NJ). EVALUATION OF ELECTROSTATIC DISCHARGE (ESD) DAMAGE TO 16k EPROMS. IITRI - EOS/ESD Symposium Proceedings, RAC Catalogue No. EOS-3, September 22-24, 1981, pp. 236-241.

D. RF EOS

For completeness a few papers treating RF generated EOS were also examined. These are listed below.

Whalen, J. J., M. L. Thorn, E. Rastefano (State University of NY at Buffalo, Amherst, NY) and M. C. Calactera (Air Force Avionics Laboratory, Wright Patterson AFB, Dayton OH). MICROWAVE NANOSECOND PULSE BURNOUT PROPERTIES OF ONE MICRON MESFETS. IITRI - EOS/ESD Symposium Proceedings, Sept. 1979, RAC Catalogue No. EOS-1, pp. 147-157.

Hewitt, H. J., and R. A. Blore (U.S. Air Force, Rome Air Development Center, Griffiss AFB, NY) and J. J. Whalen (SUNY at Buffalo). SUSCEPTIBILITY OF UHF RF TRANSISTORS TO HIGH POWER UHF SIGNALS - PART II. Rept. No. RADC-TR-76-44, Contract No. F30602-75-C-0122, April 1976, 74 pp.

Hart, A. R. (U.S. Navy, Naval Electronics Laboratory Center, Electron Material Sciences Division, San Diego, CA). RF FAILURE PREDICTION FOR MOS 4001 and 4011 INTEGRATED CIRCUITS. Rept. No. NELC R501, Code No. 4600, TN3107, January 19, 1976, 47 pp.

E. MODELING

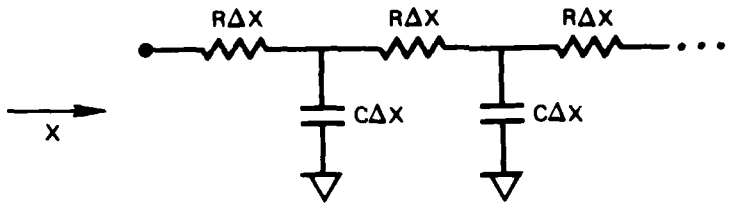
J. H. Lee, W. J. Orvis, L. C. Martin, Theoretical Modeling of EMP Effects in Semiconductor Junction Devices, AFWL-TR-82-91.

W. J. Orvis, et al, "Modeling and Testing for Second Breakdown Phenomena", Electrical Overstress/Electrostatic Discharge Symposium Proceedings, EOS-3, 1983.

APPENDIX D

PHYSICAL BASIS FOR THERMAL ANALOG NETWORKS

Consider the following RC transmission line:



$$\Delta V = IR\Delta X \Rightarrow \frac{\Delta V}{\Delta X} = IR \Rightarrow \frac{\partial V}{\partial X} = IR$$

$$\Delta I = C\Delta X \frac{\Delta V}{\Delta t} \Rightarrow \frac{\Delta I}{\Delta X} = C \frac{\Delta V}{\Delta t} \Rightarrow \frac{\partial I}{\partial X} = C \frac{\partial V}{\partial t}$$

$$\frac{\partial^2 V}{\partial X^2} = \frac{\partial}{\partial X}(IR) \Rightarrow R \frac{\partial I}{\partial X} \Rightarrow RC \frac{\partial V}{\partial t}$$

$$\left[\frac{\partial V}{\partial t} = \frac{1}{RC} \frac{\partial^2 V}{\partial X^2}\right]$$

Compare the result to the one dimensional heat flow equation:

$$\frac{\partial T}{\partial t} = C^2 \frac{\partial^2 T}{\partial X^2}$$

$$C^2 = \frac{K}{\sigma\rho}$$

where K = thermal conductivity

σ = specific heat

ρ = density

Thus: $\left[RC = 1/C^2\right]$

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